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ADVANCED DETECTORS AND SIGNAL PROCESSING FOR BUBBLE MEMORIES

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INTRODUCTION

1.1. INTRODUCTION

Recent progress in silicon on insulator (SOI) technology has made it practical to fabricate silicon devices on substrates other than single crystal silicon. In this thesis, we explore the practicality of using SOI technology to enhance the performance of bubble memories, a well established technology for high density memories. Device quality films formed by laser recrystallization could be used to fabricate magnetic field sensors on bubble chips. This is a particularly exciting application of silicon on garnet technology since replacing the magnetoresistive detectors with silicon detectors would increase the detector output signal without affecting the access time. Placing more silicon magnetic field sensors on the bubble chip would lower the memory access time; the output signal for each detector need not be compromised in the process. In fact, Fry and Hoey demonstrate that a single-crystal multi-drain field-effect magnetotransistor can have a sensitivity of 0.25V/Kgauss [1]. Lutes, Nussbaum, and Aadland demonstrate that a single-crystal magnetodiode can have a sensitivity of 4.9 V/T [2].

The use of beam recrystallization techniques to fabricate semiconductor devices is well established experimentally [3, 4, 5, 6]. Laff and Hutchins fabricated n^+-p diodes in laser recrystallized polysilicon supported by silica substrates [7]. Lee *et al.* fabricated thin film MOSFETs in laser recrystallized polysilicon supported by single crystal silicon substrates coated with silicon nitride (Si_3N_4) [4]. The work of Lee *et al.* demonstrates that high-quality crystalline silicon films can be grown on amorphous substrates: a bubble substrate coated with SiO_2 (or a silicon wafer coated with SiO_2 or

Si_3N_4) effectively acts as an amorphous substrate when one tries to grow a crystalline film on it. The excellent results obtained for MOSFETs are encouraging since Fry's magnetotransistor is fabricated using a MOSFET process. In principle then, one should be able to build magnetotransistors, MOSFETs, and other devices on bubble substrates.

Beam recrystallization is a thin film zone-melting process; it is very similar to the float-zone crystal growth technique used to grow single crystal silicon. Basically, a heat source is scanned across the surface of a fine grain polysilicon film. The area illuminated by the source is melted, and as the source is scanned away, the molten silicon freezes and hence "recrystallizes". Many workers use an argon ion laser as the heat source. The laser recrystallization process minimizes the time that the bubble film is at elevated temperatures. Although a $1\mu m$ thick SiO_2 film separates the polysilicon layer from the bubble film, this insulating film does not thermally isolate the molten silicon zone from the bubble film. Some heating of the bubble film therefore occurs. The brevity of this heating minimizes the undesirable effects of substrate/bubble film heating.

The justification for beam recrystallization is simple: recrystallized silicon films have better electrical properties than do fine grain (~500Å) polysilicon films. Films with better electrical properties are desirable since better electronic devices can be fabricated in them. A MOSFET with a higher transconductance (electron mobility) will have a higher maximum frequency of operation; a MOSFET with a smaller $|V_T|$ (absolute value of the threshold voltage) will be inherently more useful since smaller D.C. voltages are required to properly bias the device. The electron mobility for laser recrystallized silicon films is typically 170-450 $cm^2/V\text{-}S$ or better [8]; fine grain polysilicon films usually have electron mobilities on the order of 10 $cm^2/V\text{-}sec$ [9]. Threshold voltages for MOSFETs fabricated in laser recrystallized silicon are generally around a few volts (1V is common), while threshold voltages for MOSFETs fabricated in fine grain poly-Si are on the order of tens of volts (35V is not at all uncommon).

The high threshold voltages for MOSFETs fabricated in fine grain polysilicon can be understood by examining the properties of polysilicon films. Polysilicon films are known to contain a large number of deep defect levels within the forbidden gap [10, 9]; these defects act as acceptors or donors. Kamins shows that these defects affect the threshold voltage both theoretically and experimentally [8]. The threshold voltage is given by

$$V_T = \Phi_{Ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_f$$

$$- \quad - \quad (+)\text{n-channel} \quad (+)\text{n-channel} \qquad \text{Eqn. (1-1)}$$

$$- \quad - \quad (-)\text{p-channel} \quad (-)\text{p-channel}$$

where Φ_{Ms} is the work function difference between the metal and semiconductor, Q_i is an effective positive charge which models the effects of oxide and surface state charge, Q_d is the depletion region charge, C_i is the gate oxide capacitance per unit area, and ϕ_f is the surface potential required to bend the bands down to the intrinsic condition [11]. Equation (1-1) can be used for both n and p-type channel devices; the appropriate signs are indicated below this equation. Kamins demonstrates that donors and acceptors at the grain boundary can increase or decrease Q_d; this ΔQ_d affects V_T through the Q_d/C_i term.

A large density of defect states at the grain boundaries affects electron transport between the polysilicon grains: the larger the barrier ϕ_B the lower the electron flux, and this in turn implies a lower electron mobility (assuming an n-channel enhancement MOSFET). The potential barrier is given by

$$\phi_B = \frac{kT}{|q|} \ell n \frac{n_c}{n_g} \qquad \text{Eqn. (1-2)}$$

where q is the charge of an electron, k is Boltzmann's constant, T is the absolute temperature, n_c is the conduction electron density in the crystallite region, and n_g is the conduction electron density at the grain boundary [12]. Equation 1-2 is valid when the semiconductor is being inverted. The ratio n_c/n_g is a function of applied gate voltage; it will decrease with increased gate voltage when the number of defect states in the grain boundary regions is much smaller than the number of field-induced electrons. At some value of gate voltage, ϕ_B will decrease to an insignificant value; hence, the potential barrier is no longer the dominant factor affecting electron transport between grains. Lee presents experimental evidence which shows that this model accurately describes laser recrystallized polysilicon; he also shows that the intercrystalline barrier ϕ_B is always significant for fine grain polysilicon. [8]

Although there have been no reports of active semiconductor devices fabricated on garnet, some authors have studied the effects of laser [13, 14, 15, 16, 17, 18, 19] and

thermal [20, 21, 22, 23, 24, 25, 26, 27] anneals on garnet films. Schultz *et al.* have shown that laser annealing a bubble film can increase its saturation magnetization ($4\pi M_s$) by more than 100% without changing K_u significantly [13]. Similar results were reported by Herman *et al.* [15]. Suran *et al.* have shown that only the topmost surface layer of a bubble film is converted to the new value of $4\pi M_s$ if the laser power is below a critical value [14]. The mechanism responsible for producing the change in $4\pi M_s$ involves a redistribution of magnetic and nonmagnetic ions between the octahedral and tetrahedral lattice sites [13, 16]. Ando *et al.* have given vivid experimental evidence that laser annealing can reduce K_u to the point that the preferred orientation for the magnetization is no longer perpendicular to the plane of the film [19]. Ando *et al* used films with the composition $(YBi)_3(FeGa)_5O_{12}$, while Schultz used films with compositions such as $Eu_{0.6}Y_{2.4}Ga_{1.15}Fe_{3.85}O_{12}$.

Researchers [23, 13, 15, 17, 18]have investigated parts of the process required to fabricate MOSFETs on bubble substrates. The forenamed investigators were not trying to fabricate MOSFETs on bubble substrates; they were concerned with more fundamental issues. For instance, LeCraw *et al.* [23] have shown that silicon can be deposited on bubble films and subsequently heated to high temperatures (~525°C), without producing irreversible changes in $4\pi M_s$. Here we extend LeCraws work by trying to deposit polysilicon layers at 625°C without changing important magnetic properties such as $4\pi M_s$, K_u, and ℓ (characteristic length). Schultz *et al.* [13] and Herman *et al.* [15] have studied how laser annealing affects bubble films; Petek et al. [16] have shown that bubble films can momentarily withstand temperatures as high as 1400°C. Here, we extend these laser annealing studies to include bubble films coated with silicon dioxide and polysilicon layers. Our laser annealing study includes additional conventional furnace anneals to determine whether or not the laser induced changes (in $4\pi M_s$ and ℓ) can be reversed to preanneal values. Results in Chapter 2 show that garnet films can be sequentially exposed to all the temperature treatments necessary to fabricate semiconductor devices. Results in Chapter 3 show that MOSFETs of modest quality can be fabricated on bubble substrates.

CHAPTER 2
ANNEALING OF BUBBLE FILMS

In this chapter, we examine the annealing behavior of magnetic films. The first section highlights important facts about magnetic films grown on gadolinium gallium garnets. Measurement techniques are discussed in the following section. These measurement techniques are used to determine the magnetization and characteristic length for bubble films used in this work. The third section gives evidence that annealing ambients affect bubble film properties; moreover, in Section 2.4 we show that bubble films of different compositions are not equally affected by the ambient in which polysilicon is deposited. Following this, the high temperature stability of silicon-on-garnet structures is investigated. The effects of laser and post-laser anneals are studied in Sections 2.6 and 2.7. The results of this work are then used to point the way to a realistic silicon on garnet device process.

2.1. BACKGROUND

In useful magnetic bubble films, the magnetization $4\pi M_s$ tends to be oriented perpendicular to the plane of the bubble film. The preference for this orientation is described by the uniaxial anisotropy parameter K_u. The magnetization will be perpendicular to the plane of the film if K_u is greater than the demagnetization energy density $2\pi M_s^2$. Magnetostatic energy considerations determine the type of domain structure that exists in the demagnetized state; Figure 2-1(A) shows the observed domain structure. Application of a magnetic field will cause domains parallel to it to grow in size, while those anti-parallel to it will shrink (Fig. 2-1(B)). When the applied field has increased sufficiently, the anti-parallel domains will become cylindrical (Fig. 2-1(C)). These domains will exist over a range of bias fields, as dictated by the Thiele stability criteria [28]. Domains are surrounded by a magnetic transition region, called a domain wall, which has an associated width

$$\delta_w = \pi(A/K_u)^{1/2} \qquad \text{Eqn. (2-1)}$$

and energy density

$$\sigma_w = 4(AK_u)^{1/2}. \qquad \text{Eqn. (2-2)}$$

A is the exchange parameter. For the case of no applied field, the wall energy (integral of the wall energy density σ_w over the wall area) balances the magnetostatic energy when the thickness h of the bubble film is given by $h=\sigma_w/4\pi M_s^2$. This ratio is a significant dimension and is called the characteristic length, where

$$\ell \equiv \sigma_w/(4\pi M_s^2). \qquad \text{Eqn. (2-3)}$$

Combining Equations (2-2) and (2-3) gives

$$K_u = M_s^4 \ell^2 \frac{\pi^2}{A} \qquad \text{Eqn. (2-4)}$$

In the general case, Equation (2-4) is off by at most a constant.

The magnetic properties of magnetic garnet bubble films are strongly related to the crystal structures of such films. Three different types of interstices are formed by the host oxygen lattice. The garnet formula is given by

$$\langle RE_3^{3+} \rangle \, [Fe_2^{3+}] (Fe_3^{3+}) O_{12}. \qquad \text{Eqn. (2-5)}$$

<RE> indicates a dodecahedral site, surrounded by 8 oxygens and occupied by a rare earth ion. Common rare earth substitutions are Sm, Eu, Gd, Tb, Dy, Ho, Y, Er, Tm, Yb, and Lu. It is the ionic ordering of two or more of these rare earths on the dodecahedral sites in proportion to ion size differences which establishes the perpendicular anisotropy in bubble films grown on gadolinium gallium garnets. [Fe]

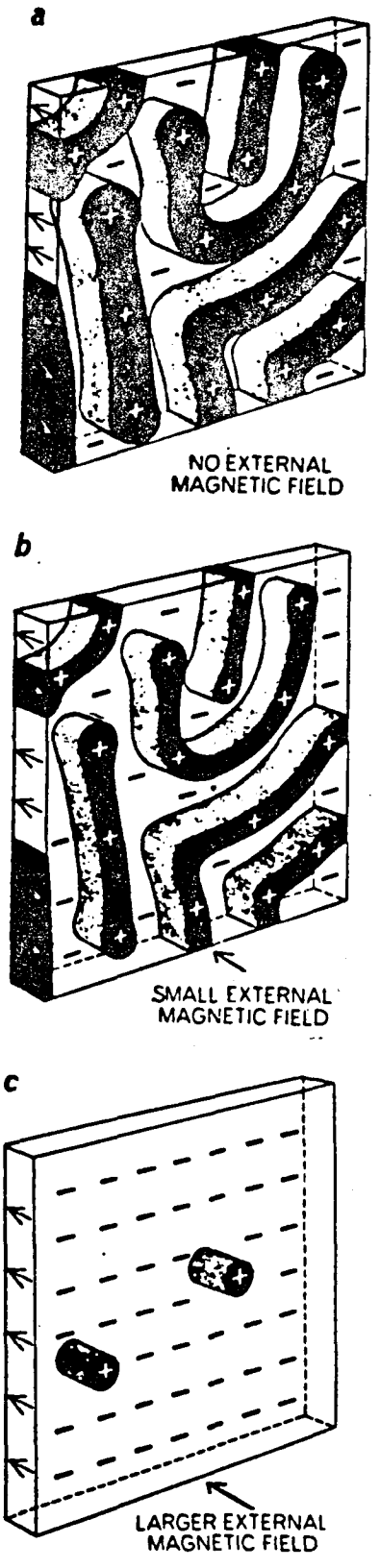


Figure 2-1: Magnetic bubble domains in thin films. After Bobeck and Scovil.

indicates an octahedral site surrounded by 6 oxygens and occupied by an iron. (Fe) indicates a tetrahedral site surrounded by 4 oxygens and occupied by an iron. The ions on the <RE>, [Fe], and (Fe) sites comprise three magnetic sublattices; the dodecahedral sublattice is parallel to the octahedral sublattice, and the octahedral sublattice is anti-parallel to the tetrahedral lattice. The total magnetization ($4\pi M_s$) is the vector sum of these three sublattice magnetizations.

It is possible to vary the magnitude of $4\pi M_s$, and hence the bubble diameter, by diluting the octahedral or tetrahedral sublattice with a nonmagnetic impurity. Gallium is one such nonmagnetic dilutant. When Ga^{3+} is substituted for Fe^{3+}, ~ 90% goes on the tetrahedral sites and ~10% goes on the octahedral sites. The actual site distribution is temperature dependent. To describe this temperature dependency, it is convenient to rewrite the garnet compositional formula with reference to the octahedral and tetrahedral sites:

$$\langle RE_3 \rangle [Fe_{2-x}Ga_x](Fe_{3-y}Ga_y)O_{12}, \qquad \text{Eqn. (2-6)}$$

where x and y are the number of Ga atoms per formula unit on the [ ] and ( ) sites, respectively. The temperature dependence of the site distribution is then given by the Borghese thermodynamic equilibrium expression [29, 13]

$$\frac{y(2-x)}{x(3-y)} = \exp\left(\frac{E_s}{kT}\right), \qquad \text{Eqn. (2-7)}$$

where k is the Boltzmann constant, T is the absolute temperature, and E_s is an energy which describes the preference of Ga atoms for the tetrahedral sites. Consequently, $4\pi M_s$ can be adjusted by thermal annealing: the bubble film is annealed at a temperature T until a well defined equilibrium distribution of Ga is achieved, then the bubble film is cooled to room temperature to quench in the equilibrium distribution.

2.2. MAGNETIC MEASUREMENTS

Details of the magnetic measurements used to determine $4\pi M$ and ℓ are given in Appendix A for the interested reader. At this point, it will be sufficient to state that the $4\pi M_s$ and ℓ data were calculated from measurements of the stripe domain width, $(0.5\ P_o)$, the bubble collapse field, (H_o), and the bubble film thickness (h) [30]. The thickness of the bubble film was measured using an optical interference technique.

2.3. AMBIENT EFFECTS

2.3.1. Changes In $4\pi M_s$

The first furnace anneals were designed to provide data on how annealing ambients affect bubble films. Nitrogen anneals were conducted with samples having the structure shown in Fig. 2-2(A); oxygen anneals were conducted with samples having the structure shown in Fig. 2-2(B). The results for film A $[(Sm_{0.35}Gd_{0.55}Tm_{1.22}Y_{0.9})(Fe_{4.61}Ga_{0.25}Al_{0.14})O_{12}]$ are shown in Fig. 2-3. All anneals were 30 minutes in duration and were conducted in a noncumulative fashion; that is, each sample was used for only one anneal. Anneals in nitrogen produced major changes in the saturation magnetization $(4\pi M_s)$ for temperatures near 1100°C. Nitrogen anneals at 1230°C proved to be very harmful to the bubble film; after the anneal, it was not possible to measure $4\pi M_s$ for the film. Oxygen anneals in the same 1100-1230°C range were not nearly as damaging.

2.3.2. K_u Data

Table 2-1 lists the values of $(4\pi M_s)^4\ell^2$ before and after annealing. This table was constructed using the data in Fig. 2-3 and the corresponding characteristic length data, which is not included in this thesis. The columns labeled $\Delta(4\pi M_s)^4\ell^2$ show how the uniaxial anisotropy changes since

$$K_u \propto (4\pi M_s)^4\ell^2 \qquad \text{Eqn. (2-8)}$$

in the general case. Data in this table show that K_u decreases significantly if the bubble film is annealed at very high temperatures. K_u decreases by a factor of three when the bubble film is annealed in nitrogen at 1127°C and K_u decreases by a factor

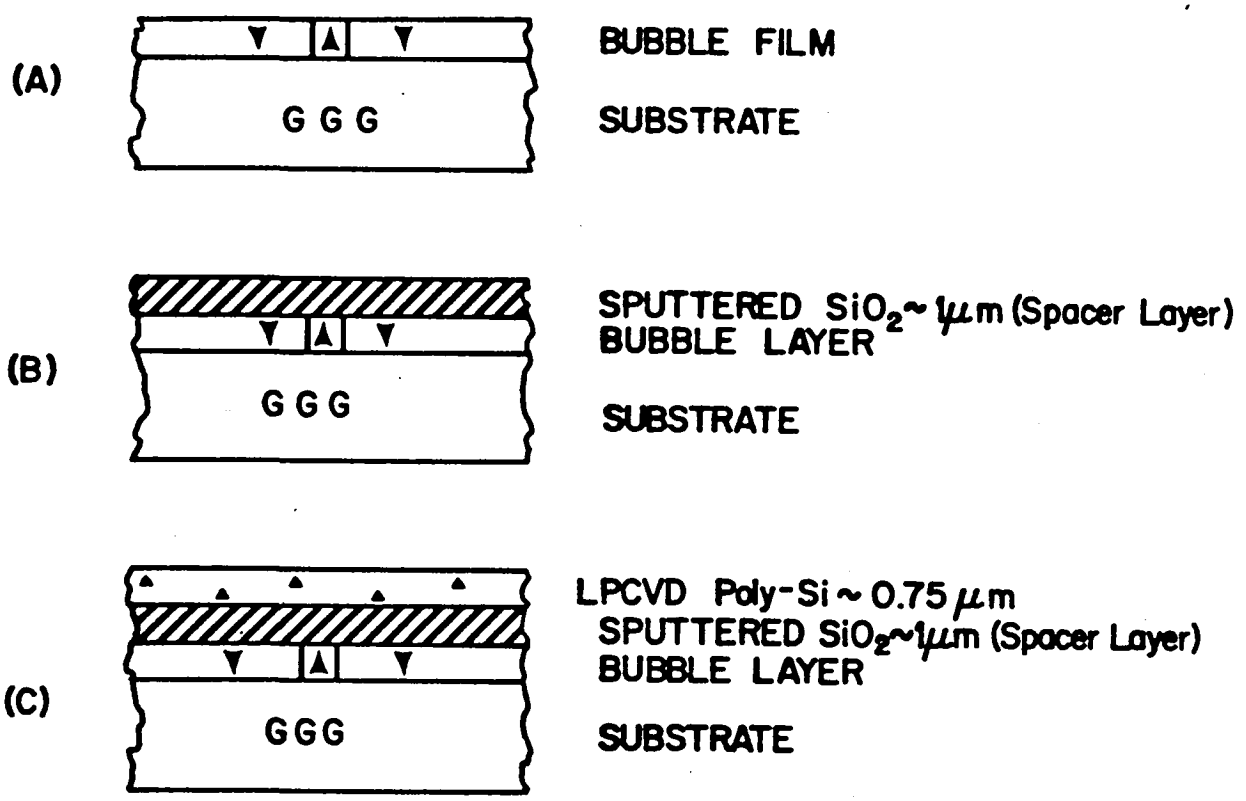


Figure 2-2: Cross sections of samples used for bubble film annealing experiments.

of two when the bubble film is annealed in oxygen at 1234°C. The overall trend is that K_u decreases, even though there is substantial scatter in the data. It is the author's opinion that, scatter in the K_u data is an artifact of the measurement techniques used to determine $4\pi M_s$ and ℓ (see Section 2.8 for more details).

2.4. POLYSILICON DEPOSITION

Low pressure chemical vapor deposition (LPCVD) is used to deposit the polysilicon layer shown in Fig. 2-2(C) since this technique produces the highest quality films. However, LPCVD is a high temperature process, and, for this reason, an annealing experiment was conducted. The experiment dealt with two films, film A and film B $[(Sm_{0.3}Gd_{0.4}Tm_{0.73}Y_{1.57})(Fe_{4.6}Ga_{0.4})O_{12}]$. Basically, the experiment involved depositing $0.75\mu m$ of polysilicon on the substrate shown in Fig. 2-2(B). The saturation magnetization and characteristic length for each film was measured before and after the polysilicon deposition. The results for film A are: before the polysilicon deposition $4\pi M_s$=633gauss and ℓ=0.1737μm; after the polysilicon deposition $4\pi M_s$=547gauss and ℓ=0.1961μm. The results for film B are: before the polysilicon deposition $4\pi M_s$=687gauss

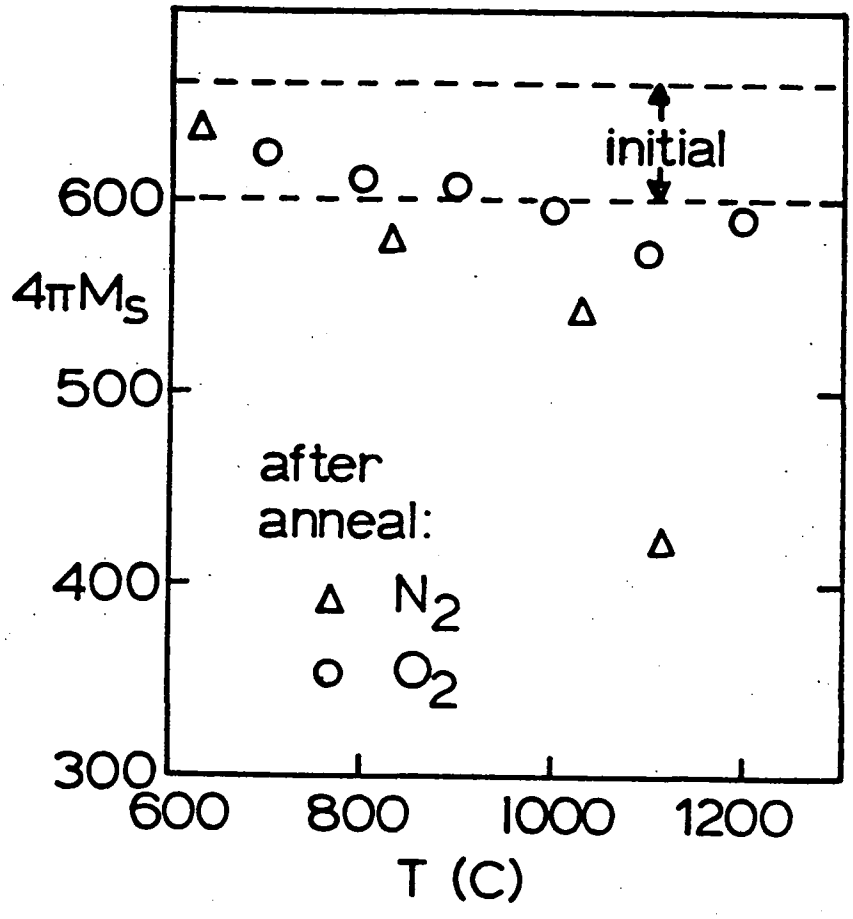


Figure 2-3: $4\pi M_s$ after annealing at T °C for 30 min. in nitrogen or oxygen. Dotted lines show the interval in which preanneal $4\pi M_s$ measurements fell.

and ℓ=0.113μm; after the polysilicon deposition $4\pi M_s$=691gauss and ℓ=0.1269μm. It is apparent that the polysilicon deposition does not equally affect films A and B, with film A experiencing the larger change in $4\pi M_s$.

2.5. HIGH TEMPERATURE STABILITY

MOSFET gate oxides are usually grown above 800°C; consequently, the chemical stability of the silicon on garnet material system is important at high temperatures (700–1200°C). Interesting results are obtained when the structure shown in Fig. 2-2(C) is annealed. Oxygen anneals at 1100°C initiate the growth of large irregularly shaped crystalline deposits on film A: they consist of a labyrinth of iron-rich hexagonally-symmetric spike-like protrusions, like those shown in Fig. 2-4. Fig. 2-5 shows the results of energy-dispersive X-ray analysis for a typical crystalline deposit. The

O_2 Anneals of Film A

Temp °C	$\frac{(4\pi M_s)^4 \ell^2}{10^9}$ Before	$\frac{(4\pi M_s)\ \ell^2}{10^9}$ After	$\frac{\Delta(4\pi M_s)^4\ \ell^2}{10^9}$
700	4.0	4.4	+0.4
800	5.0	4.1	+0.9
900	4.1	3.9	+0.2
1000	5.1	4.1	+1.0
1100	4.8	3.4	+1.4
1127	3.9	4.4	+0.5
1234	4.2	2.1	+2.2

N_2 Anneals of Film A

Temp °C	$\frac{(4\pi M_s)^4 \ell^2}{10^9}$ Before	$\frac{(4\pi M_s)^4\ \ell^2}{10^9}$ After	$\frac{\Delta(4\pi M_s)^4\ \ell^2}{10^9}$
628	5.0	4.5	+0.5
833	2.8	4.1	+1.3
1034	4.0	3.1	+0.9
1127	3.7	1.2	+2.5
1230	2.8	-	-

Table 2-1: $(4\pi M_s)^4\ell^2$ vs. annealing temperature for oxygen and nitrogen ambients.

energy-dispersive X-ray spectrometer used to take the spectrum was an attachment to the SEM used to take the micrograph shown in Fig. 2-4; the SEM was operated at an accelerating voltage of 25 KeV. Figure 2-6 shows a spectrum taken on the silicon film adjacent to the large deposit. From these two X-ray spectrums it is clear that the deposits are indeed iron rich. The crystalline deposits are absent if the oxygen anneal is conducted below 1000°C; furthermore, the difference between the pre- and post-anneal $4\pi M_s$ values is quite small (less than ~25gauss).

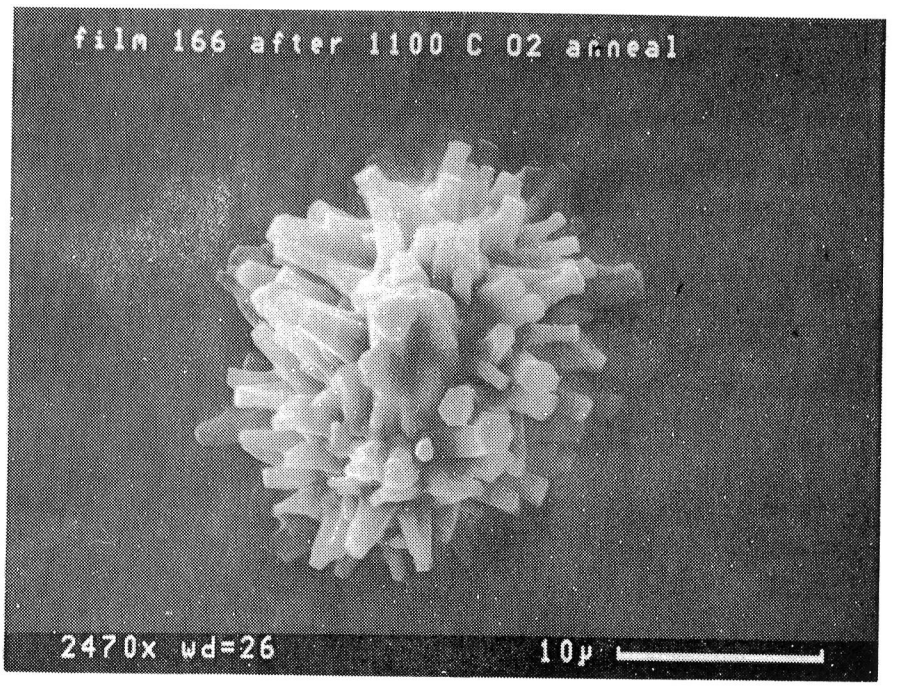


Figure 2-4: Iron rich crystalline deposits on film A after a 30 min. oxygen anneal at 1100°C.

2.6. LASER ANNEALS

An argon laser, operating with all visible lines, is used to recrystallize the 0.75μm polysilicon layer shown in Fig. 2-2(C). The light beam is focused to a 30μm spot size, and this beam is scanned in a raster pattern at a speed of 5cm/sec, with a line to line separation of 15μm. The substrate is kept at 400°C during the recrystallization (laser anneal). With this setup, the power required to recrystallize the polysilicon film - without melting the bubble film - is generally 0.7±0.1W. For this power, the typical silicon grain size is 5x20μm.

The 0.7±0.1W laser anneals were found to affect bubble film B. Before the laser annealing $4\pi M_s$ was 695 gauss and after the laser annealing $4\pi M_s$ was 774 gauss. The characteristic length was 0.1118μm before the laser annealing and was 0.0924μm after the laser anneal. These data are summarized in Table 2-2. Figure 2-7 shows that the bubble collapse field increased significantly in the laser annealed area (LA stands for laser annealed, and NLA stands for not laser annealed). In addition, it was found that the domains in the bubble films exhibited some preference to align parallel to the scan direction of the laser beam after the laser anneal.

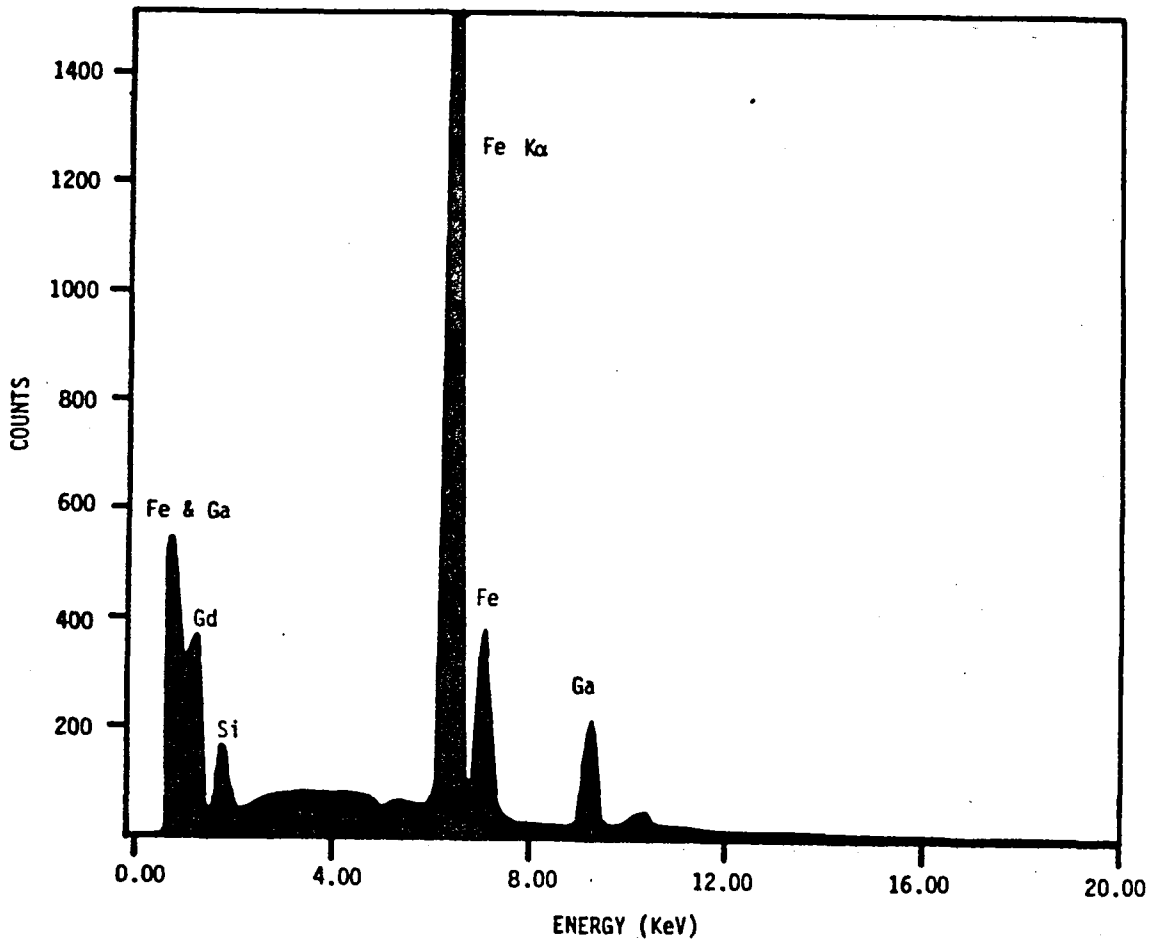


Figure 2-5: Energy-dispersive X-ray spectrum of the crystalline deposit shown in Fig. 2-4.

2.7. POST-LASER ANNEALS

The recovery of laser induced changes in $4\pi M_s$ is investigated in the last experiment. Laser annealed samples of film B, with the structure shown in Fig. 2-2(C) were annealed in oxygen at a temperature of 850°C for times between 5 and 40 minutes. Figure 2-8 shows that post-laser anneals between 5 and 40 minutes in length at 850°C restore the magnetization to nearly its as-grown value. The dashed lines in this figure indicate the range of measured $4\pi M_s$ values in the areas which were not laser annealed. Actually, a 5 min. post-laser anneal is all that is necessary to insure that $4\pi M_s$ in the laser annealed areas matches $4\pi M_s$ in the non-laser annealed areas. However, the tendency of $4\pi M_s$ to remain near the 5 min. post-laser anneal value is very important to the success of silicon on garnet technology. This stability of $4\pi M_s$ for longer annealing times allows the gate oxide thickness for MOSFETs on garnet substrates to vary between ~100 and ~2000 Å. These values are calculated from

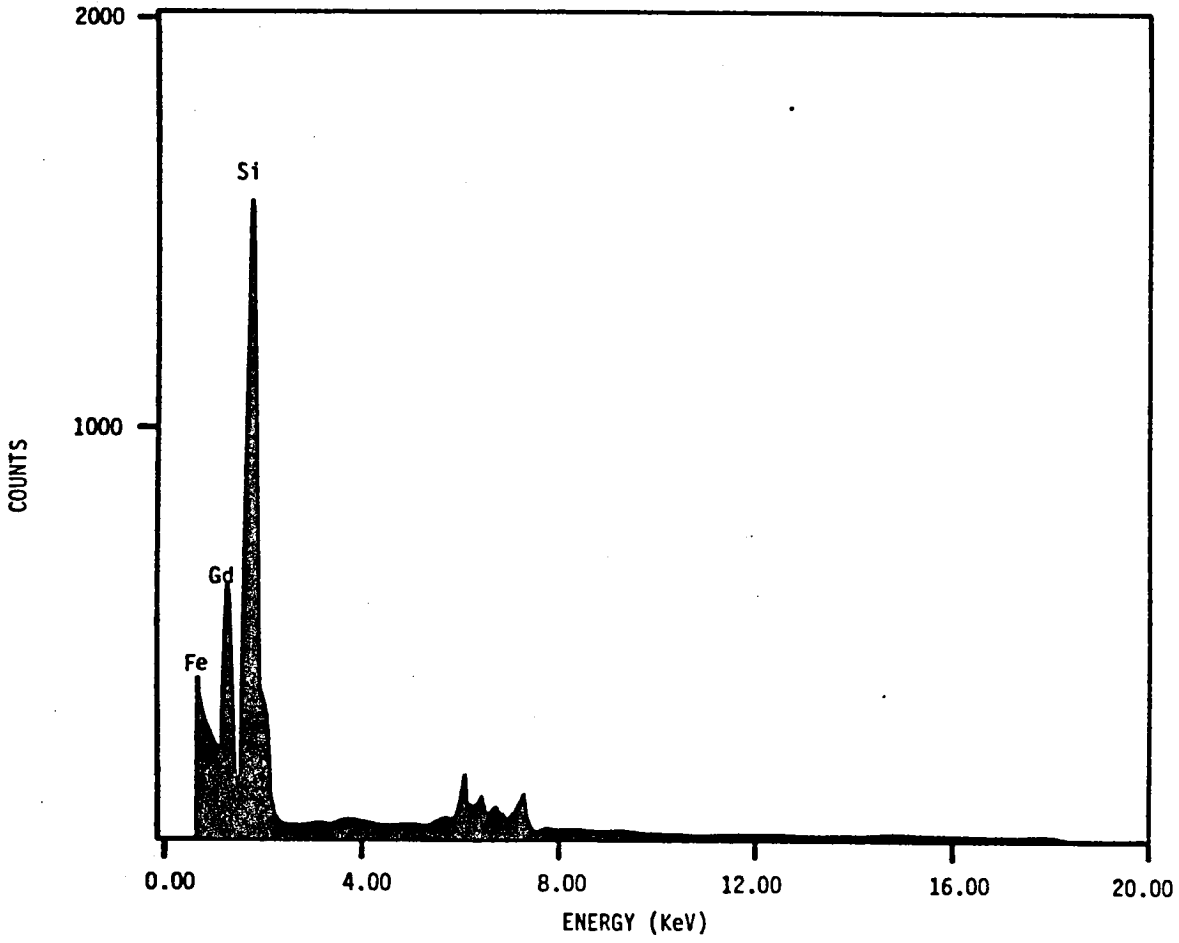


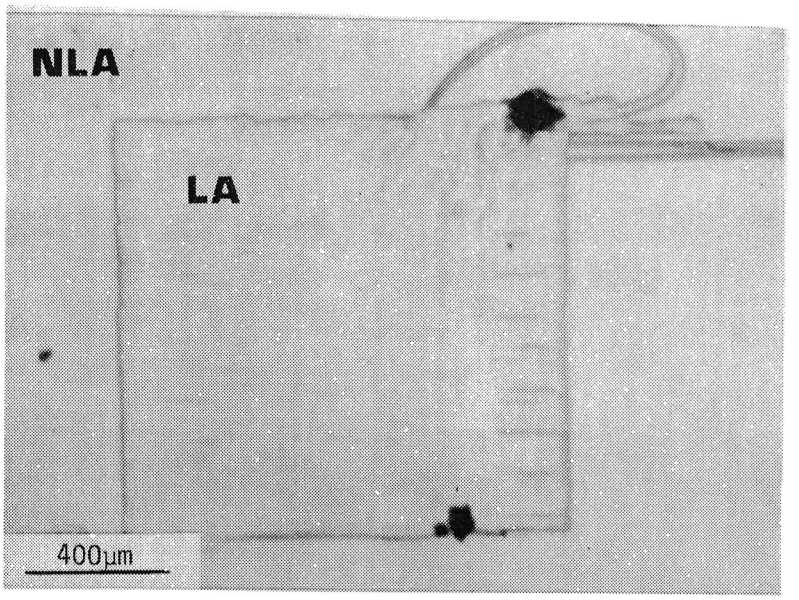
Figure 2-6: Energy-dispersive X-ray spectrum of an area adjacent to the crystalline deposit shown in Fig. 2-4.

$$\log t_{ox} = 0.8617 \log + 1.4265, \; 5 \text{ min.} < t < 150 \text{ min.} \qquad \text{Eqn. (2-9)}$$

where t_{ox} is the thickness of the gate SiO_2 in angstroms and t is the time in minutes of the 850°C steam oxidation. Note that we determined this oxidation characteristic experimentally; the oxidation process is considered in a number of integrated circuit engineering texts such as the one by Hamilton and Howard [31].

	$4\pi M_s$	ℓ	$\frac{(4\pi M_s)^4 \ell^2}{10^9}$
Laser Annealed Areas (5 samples)	774 ± 17	0.0924 ± 0.0049	3.1 ± 0.6
Areas Not Laser Annealed (5 samples)	674 ± 20	0.1219 ± 0.0068	3.1 ± 0.7
As Grown (1 sample)	695 ± 22	0.1118 1 0.0097	2.9

Table 2-2: $4\pi M_s$, ℓ and $(4\pi M_s)^4 \ell^2$ for as grown and laser annealed material. The data for "areas not laser annealed" correspond to the NLA areas shown in Fig. 2-7. The data for the "laser annealed areas" correspond to the LA areas shown in Fig. 2-7.



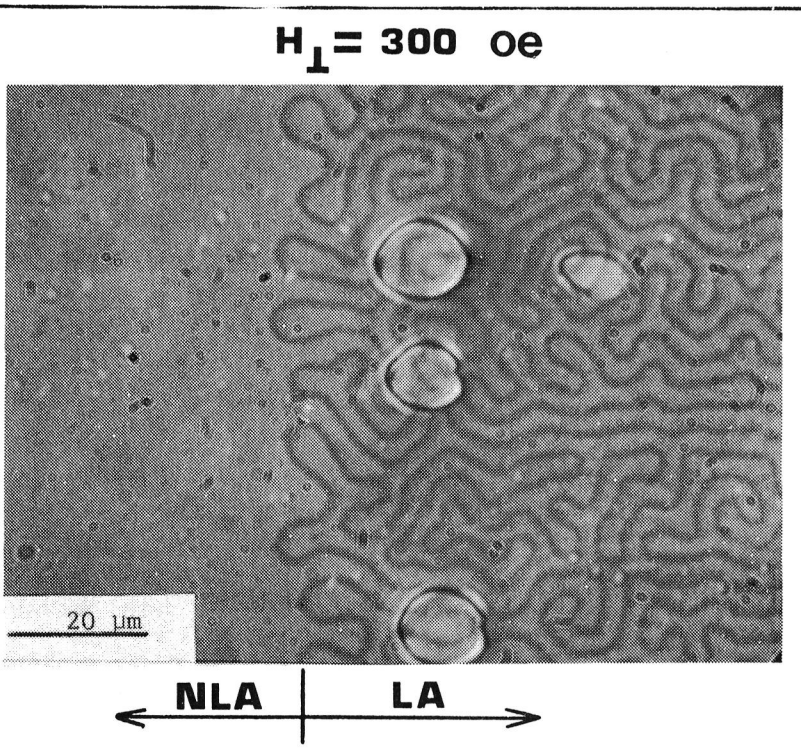


Figure 2-7: Top photograph shows the surface view of the structure shown in Fig. 2-2(C) after recrystallization; the sample was capped with 1μm of sputtered oxide during recrystallization. LA indicates that the region was laser annealed and NLA indicates that the region of interest was not laser annealed. Bottom photograph shows the transition between LA and NLA areas with a 300 oe perpendicular bias field applied.

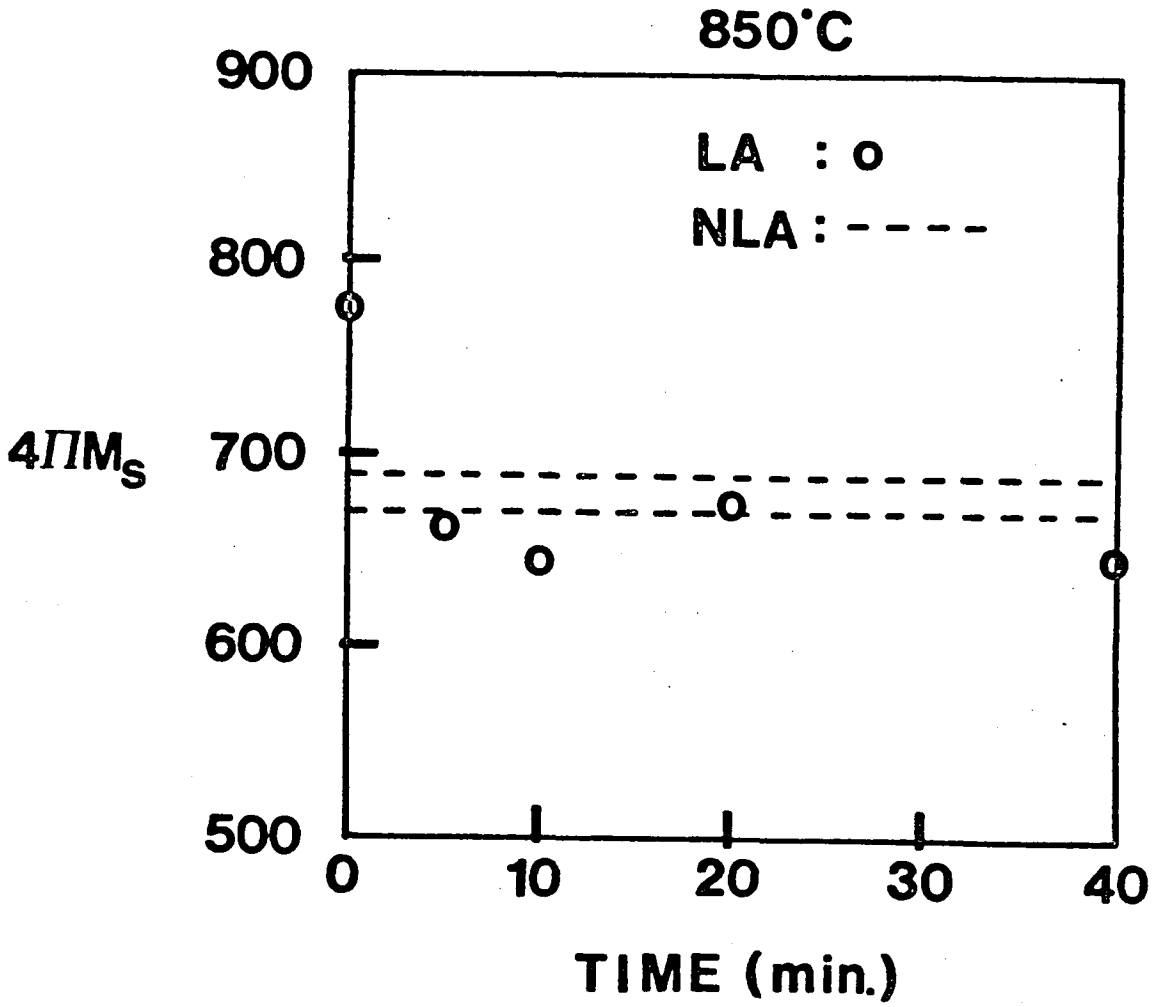


Figure 2-8: $4\pi M_s$ after post-laser annealing in oxygen at 850°C for the indicated times. LA and NLA indicate that the data is for the areas shown in Fig. 2-7. The dotted lines indicate the interval in which NLA $4\pi M_s$ measurements fell.

2.8. DISCUSSION

Figure 2-3 shows that changes in $4\pi M_s$ are a strong function of the ambient used during the anneal; changes occur at a much lower temperature during nitrogen anneals than during oxygen anneals. A mechanism that explains these changes is now discussed. During a nitrogen or oxygen anneal, a transfer of Ga, Al, and Fe takes place between the tetrahedral and the octahedral lattice sites, and it is this transfer which produces the observed change in $4\pi M_s$, [25, 20]. We suggest that oxygen can escape from the

bubble film when it is annealed in a nitrogen ambient. The oxygen vacancies or the resultant Fe^{2+} ions formed during the nitrogen anneal accelerate the cation transfer with respect to an identical oxygen anneal [23]. A faster cation transfer rate in turn implies a larger $\Delta 4\pi M_s$ for any given anneal.

The observed behavior of K_u, which may be obtained from Table 2-1 and Eqn. (2-4), indicates that there is a reordering of the ions on the garnet dodecahedral sites. The reordering becomes significant for nitrogen anneals above ~1127°C and for oxygen anneals above ~1234°C. The degree of reordering is difficult to ascertain since the $\Delta(4\pi M_s)^4\ell^2$ values should not be both positive and negative. We attribute the large standard deviation, as well as the + and - $\Delta(4\pi M_s)^4\ell^2$ values, to the difficulty in measuring $4\pi M_s$ and ℓ for the same film before and after the anneal. The samples used had bubble films on both the top and bottom surfaces of the substrate, and no special effort was made to differentiate them. Hence, it could happen that the $+\Delta(4\pi M_s)^4\ell^2$ values result as a consequence of making measurements on the top film before the anneal and making measurements on the bottom film after the anneal or vice versa. The error in P_o/h that results from this is compounded by the fact that a small uncertainty in P_o/h transforms into a much larger uncertainty in $H_o/4\pi M_s$ (see Fig. 2-9 and note typical values for P_o/h are ~ 2.2 for film A).

A cation transfer mechanism can also be used to explain why the polysilicon deposition does not equally affect films A and B. We suggest that the larger $\Delta 4\pi M_s$ value for film A results because less energy is required to transfer the Al ion, which is smaller than the Ga ion, between the tetrahedral and octahedral lattice sites. Probably this anneal has a greater effect than nitrogen anneals at the same temperature because hydrogen liberated during the polysilicon deposition acts as a reducing agent. The accelerated cation transfer rate suggested in [23] is also plausible here since the conditions used to deposit the polysilicon (T=898°K and $t \cong 60$ min.) insure that the diffusion length

$$L = (Dt)^{1/2} \qquad \text{Eqn. (2-10)}$$

for oxygen vacancies is a significant fraction of the bubble film thickness (h=1.3 μm typically). To see this, use Metselaar and Larsen's expression

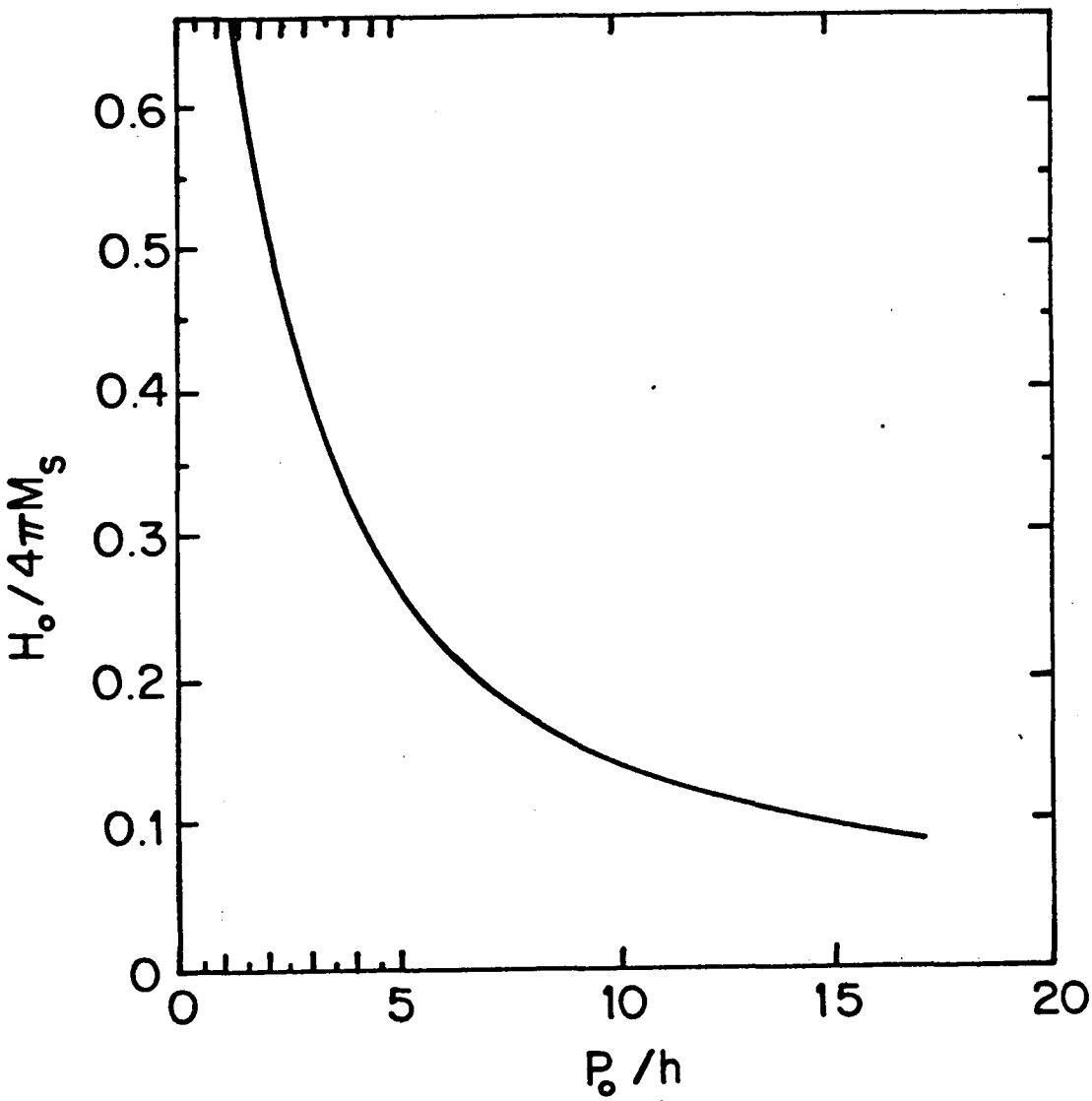


Figure 2-9: Bubble collapse field, H_o, divided by $4\pi M_s$ vs. strip domain period, P_o, at H=0 divided by thickness, h. After Fowlis and Copeland.

$$D = 8400 \exp\left(\frac{-Q}{kT}\right) \text{ cm}^2\text{s}^{-1}, \qquad \text{Eqn. (2-11)}$$

with Q= 2.9 ± 0.1 eV, k = 8.6174 x 10^{-5} eV/°K, and T = 898°K [32].

At present, the chemistry behind the formation of the crystalline deposits shown in Fig. 2-4 is not well understood. A tentative explanation is that oxide pinholes place the silicon layer in contact with the bubble film, and at 1100°C this contact allows the bubble film to react with the silicon layer. The large difference in X-ray intensities for

the Fe Kα line of the on-and off-crystallite spectra (see Figs. 2-5 and 2-6) indicates that the X-ray probe is not merely looking at the GGG substrate or bubble film. The fact that these spike-like crystalline protrusions do not appear uniformly over the sample's surface indicates that random defects exist in the undensified sputtered SiO_2 layer. Rasky *et al.* show that oxide pinholes in laterally seeded silicon-on-insulator films act as nucleation sites for macroscopic defects [33]. In addition, long annealing times at high temperatures have been shown by one author to produce large prism shaped crystallites on bubble films [24].

The laser induced behavior of $4\pi M_s$, K_u and ℓ can be explained by applying the ion redistribution mechanisms reported in the literature [16, 13]. The $4\pi M_s$ and ℓ values measured before and after the laser annealing imply that K_u does not change as a result of the laser recrystallization process since $K_u \propto \ell^2 M_s^4$. The independence of K_u implies that redistribution of the dodecahedral rare earths is not significant. Hence, a change in $4\pi M_s$ only involves a redistribution of Ga^{3+} and Fe^{3+} between the tetrahedral [d] and octahedral [a] lattice sites, with the relative change, $[\Delta 4\pi M_s / 4\pi M_s^{\text{prelaser anneal}}]$, being smaller for a bubble film with a lower gallium content [25].

Laser recrystallization of the poly-Si layer causes randomization of Ga^{3+} and Fe^{3+} ions between the [a] and [d] sites. The randomized distribution of Ga^{3+} and Fe^{3+} is quenched in due to the short dwell time of the scanning laser beam. The quenched Ga^{3+} distribution is very stable at room temperature; however, the laser induced quenched state is only metastable with respect to site preference energy considerations. These considerations dictate the preferred Ga^{3+} sublattice sites to be the tetrahedral interstices.

Results presented in Section 2.7, as well as results of other researchers [13], indicate that the metastability can be removed by a conventional furnace anneal (i.e. post-laser anneal) if the anneal is done near the bubble film's growth temperature. The optimal post-laser anneal temperature for film B is 850°C (this film is grown at 833°C). The length of this post-laser anneal is at least five orders of magnitude longer than a typical laser anneal; consequently, the Ga^{3+} ions have enough time during the post-laser anneal to assume a distribution (between [a] and [d] sites) based on site preference energy considerations. The redistribution process is thermally driven and each post-laser annealing temperature will produce a different distribution of Ga^{3+} between the [a] and [d] sites. Theory indicates that the post-laser anneal Ga^{3+} distribution can be identical with the as grown Ga^{3+} distribution [25, 34]. However,

there are limits to the reversibility; K_u actually decreases if inappropriate post-laser annealing conditions are chosen. The consequence of this is that high temperature semiconductor processing steps must be reduced to the minimum number necessary.

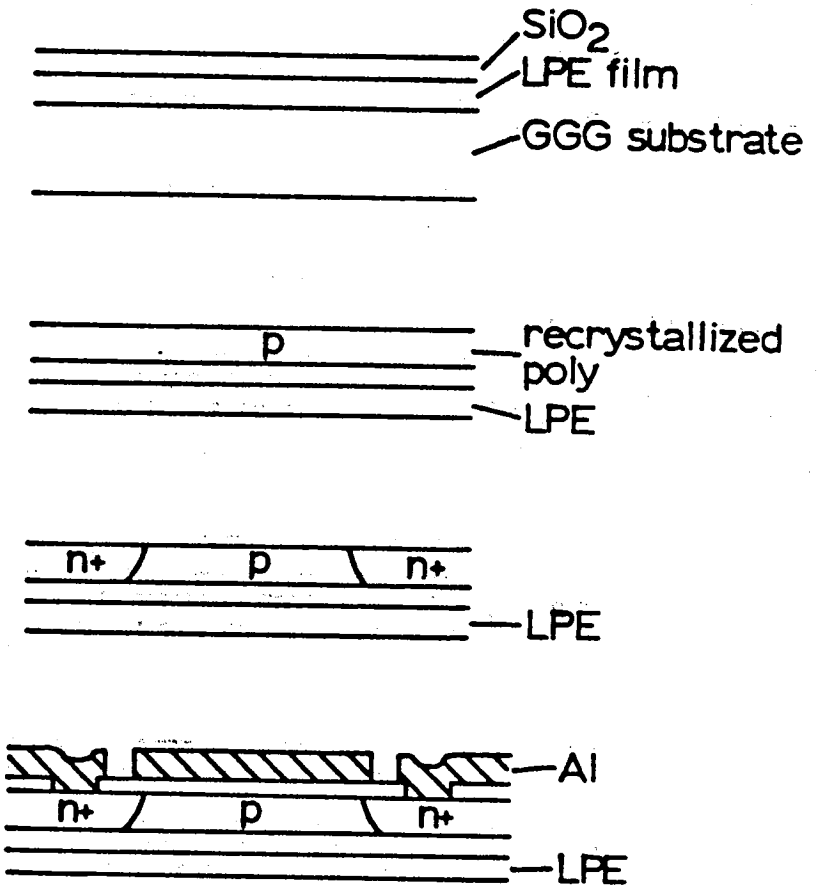


Figure 2-10: Abridged silicon-on-garnet process flow.

A process to fabricate silicon devices on bubble substrates has grown out of the annealing data presented in Sections 2.3 to 2.7. It requires only one high temperature step after laser recrystallization. The process is outlined in Fig. 2-10 and requires the following steps: (1) deposition of a 1μm thick sputtered SiO_2 spacer layer, (2) low pressure chemical vapor deposition of a 0.75μm thick small-grain polysilicon layer, (3)

laser recrystallization of the polysilicon layer, and (4) a 5-40 min. oxygen post-laser anneal. MOSFETs can be fabricated in this process if: the p-channel implant is performed immediately after step (2), the source/drain implant is performed immediately after step (3), and the gate oxide is grown during step (4). In the end, the bubble film properties, $4\pi M_s$ and ℓ, are nearly identical to those of virgin material if the process temperatures are properly selected.

CHAPTER 3
SEMICONDUCTOR DEVICES

In this chapter, we examine the structural and electrical characteristics of laser recrystallized silicon-on-garnet films. Section 3-1 introduces the characterization techniques used throughout this work; it explains why the techniques were chosen and what information can be extracted by using them. Device fabrication processes and structures are introduced in Section 3.2. Section 3.3 deals with the surface morphology of recrystallized silicon films. This is important since structural characteristics strongly influence the electrical parameters of silicon devices. The effects of antireflective recrystallization caps are briefly discussed in Section 3.4. A theory which explains the types of anomalous behavior exhibited by our MOSFETs is developed in Section 3.5. The following section then shows that our metal-semiconductor contacts are non-ohmic. Section 3-7 compares the quality of spacer layers; the spacer layers are either sputtered SiO_2 or thermally grown SiO_2. Finally, Section 3-8 characterizes MOSFETs built on magnetic bubble substrates; a discussion of particularly important results is subsequently given in Section 3-9.

3.1. CHARACTERIZATION THEORY

MOSFETs were chosen as the primary test vehicle for silicon on garnet technology since MOSFET parameters - such as μ_n, V_T, I_D^{leak}, I_G^{leak} - provide a wealth of information concerning the overall quality of laser recrystallized films. The mobility of majority carriers, μ_n (for an n-channel FET), and the threshold voltage, V_T, reveal information about the structure of the silicon film. For instance, a low V_T and high μ_n are indicative of large grain (5 x 20 μm) device-quality silicon films. In contrast, a high V_T and low μ_n are indicative of small grain (~500 Å) polysilicon films; these films, in general, exhibit much poorer device characteristics than do single crystal (or

large grain) silicon films. The drain to source current at $V_{GS} < V_T$, I_D^{leak}, can indicate that there are a number of anomalies associated with the device. If the channel length is on the order of 5 μm or less, I_D^{leak} may indicate the extent of drain to source pipelining; that is, the formation of n-type conducting filaments in the channel between the source and drain. Drain to source pipelines typically correspond to grain boundaries which connect the source and drain. This is easily understood since grain boundaries are a highly disordered state of the crystalline lattice and this disorder can lead to enhanced impurity diffusion rates. Phosphorus is known to diffuse $\sim$ 10-50 times faster along grain boundaries than it does in single crystal Si [35]. It is also possible that a conductance exists in parallel with the gate induced channel; this parallel conductance would then provide an additional current path between the source and drain different from the drain to source pipelines. The gate leakage current at V_{DS} = 0 V, I_G^{leak} indicates the integrity of the gate oxide. A leaky gate, one with a large gate leakage current (I_G^{leak} > 20 pA), might indicate the presence of trap levels within the oxide bandgap. These trap levels will allow carriers (electrons) to tunnel from semiconductor to oxide and from oxide to metal, thereby causing a gate current.

The transfer characteristic of a MOSFET provides a convenient way to determine μ_n and V_T. The transfer curve is described by

$$I_D = \left(\frac{\mu_n C_{ox} W}{2L} \right) \left(V_{GS}-V_T \right)^2 \quad \text{for} \quad |V_{DS}| > |V_{GS}-V_T|. \qquad \text{Eqn. (3-1)}$$

where W/L is the width to length ratio of the MOSFET's channel, and $C_{ox} = \epsilon_{SiO_2}/t_{ox}$ is the capacitance per unit area of the oxide layer. Note that according to Eqn. (3-1) I_D remains constant for $|V_{DS}| > |V_{GS}-V_T|$. Taking I_D to be a constant in the saturation region ($|V_{DS}| > |V_{GS}-V_T|$) is typically a good approximation. Equation (3-1) can be rewritten as

$$I_D^{1/2} = \left(\frac{\mu_n C_{ox}}{2} \frac{W}{L} \right)^{1/2} \left(V_{GS}-V_T \right). \qquad \text{Eqn. (3-2)}$$

Hence, the mobility (μ_n) can be found from the slope of $I_D^{1/2}$ vs. V_{GS}. In this thesis, all field effect mobilities are determined from $I_D^{1/2}$ vs. V_{GS} plots taken at V_{DS}=5 V. Typically the slope is determined from the line of best fit to the transfer characteristic

and the threshold voltage (V_T) is taken as the intercept of this line with the V_{GS} axis. In practice, some drain to source leakage current exists and, $I_D^{1/2}$ in Eqn. (3-2) should be replaced by $(I_D - I_D^{leak})^{1/2}$ so that all devices might be compared at the same value of induced carrier concentration and at approximately the same value of surface potential. Kamins used a similar modification in his paper to correct for the effect of parasitic parallel conductances in his MOSFETs [36].

Two alternative measurements can be made which also give μ_n and V_T. The first one is suggested by

$$g_m(sat) = \frac{\partial_D(sat)}{\partial V_G} = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T) \qquad \text{Eqn. (3-3)}$$

where $g_m(sat)$ is the transconductance in the saturation region. The second one is suggested by

$$g(\text{linear region}) = \frac{\partial I_D}{\partial V_D} = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T) \qquad \text{Eqn. (3-4)}$$

where g(linear region) is the conductance of the channel in the linear region: it is simply the slope of the I_D vs. V_D curve near the origin. In fact, Muller and Kamins [37] show that this is the preferred method to find μ_n due to the inaccuracy of the model used to derive Eqn. (3-1).

3.2. DEVICE PROCESSES AND STRUCTURES

The process that we used to fabricate MOSFETs on bubble substrates (GGG wafers with a magnetic epitaxial layer) differed significantly from the processes typically used to fabricate MOSFETs on more conventional substrates. For this reason, we shall now describe our silicon-on-garnet process in some detail. Four variations of the process are outlined in Fig. 3-1. All of the devices discussed in this chapter are fabricated on silicon or magnetic bubble substrates (Fig. 3-1(A)). The devices are separated from the substrate by a 1 μm thick spacer layer (Fig. 3-1(B)); this spacer layer is either thermally grown or sputtered SiO_2. A 0.75 μm polysilicon layer is deposited on the SiO_2 spacer by low pressure chemical vapor deposition (LPCVD). Figure 3-1(C) shows the cross sections after this step. Antireflective SiO_2 layers are

next grown or deposited on the structures (Fig. 3-1(D)). The 1/4 λ capping layer is thermally grown from the polysilicon film and the 3λ caps are sputter deposited. Following the capping process, the polysilicon layers are recrystallized using an argon ion laser (Fig. 3-1(E)). The capping layers are removed after laser recrystallization by etching in buffered HF acid. Next, a SiO_2 masking layer is grown and the locations of device islands are defined photolithographically (Fig. 3-1(F)). The SiO_2 not covered by photoresist is etched off in buffered HF (Fig. 3-1(G)). Following the mask oxide etch, the photoresist is removed in acetone; the resulting structure is shown in Fig. 3-1(H). Islands of recrystallized silicon, 25 μm x 100 μm in size, are formed by etching the exposed silicon in a solution of HNO_3, HF, and H_2O (Fig. 3-1(I)). Subsequently, the masking oxide is removed and a new SiO_2 layer is grown; this oxide layer protects the Si islands during the forthcoming ion implants. Boron, a p-type impurity in Si, is added to the silicon islands via ion implantation (Fig. 3-1(J)). Phosphorus, an n-type impurity in Si, is next added to the silicon islands via ion implantation; the p-type channel is protected from the n^+ implant by the masking photoresist (Fig. 3-1(K)). Next, the photoresist and implant oxide are removed; a high quality gate oxide is then grown in a steam ambient. Contact windows are defined using photolithography and are opened to the n^+ Si regions during a HF etch. Aluminum is then deposited via evaporation (Fig. 3-1(L)), and patterned photolithographically into source, gate and drain electrodes (Fig. 3-1(M)), thus completing the fabrication process.

Successful demonstration of a new device technology, like silicon-on-garnet, is often a complex and difficult task. The process variations outlined in Fig. 3-1 and discussed in the last paragraph are necessary to isolate potential process problems. The thermal/sputtered SiO_2 spacer variation (Fig. 3-1(D), substrate types B and C) allows one to judge the suitability of sputtered SiO_2 spacer layers without having to untangle the effects of other process steps. The thermal/sputtered SiO_2 capping layer variation (Fig. 3-1(D), substrate types A and B) allows one to determine how capping layers affect the structural and electrical properties of MOSFETs without having to consider the effects of other process steps. Likewise, one can fairly compare MOSFETs fabricated on bubble substrates to those fabricated on silicon substrates by comparing the devices fabricated on substrate types C and D (Fig. 3-1(D)). Substrate type-E was used to a limited extent in the capping layer study and is included in Fig. 3-1(D) for the sake of completeness.

3.3. SURFACE MORPHOLOGY OF RECRYSTALLIZED Si FILMS

Samples having the structures shown in Fig. 3-1(D) were prepared in the manner described in Section 3.2. The polysilicon layers were next laser recrystallized. Capping layers were removed and the flatness of each recrystallized silicon film was measured using a Dektak surface-profile measuring system.

It was found that the flatness of the recrystallized film strongly depends on the capping layer used during the recrystallization. Films recrystallized with thermally grown 1/4 λ SiO_2 caps have surface roughness values on the order of ± 0.35 μm; surprisingly the films are still continuous. Figure 3-2(C) shows the ripple like texture of such a film; Figure 3-2(D) shows the characteristic dewetting associated with thermal SiO_2 at higher laser powers. Very flat recrystallized films are obtained if the polysilicon layer is capped, as in Figure 3-1(D) (substrate types B, C and D), with a 1 μm thick sputtered SiO_2 during the recrystallization. Surface roughness is usually $\pm$ 0.01 μm, although values of $\pm$ 0.02 μm are occasionally obtained if the top oxide layer is absent (Figure 3-1(D), substrate type-E). Figure 3-2(B) shows one such film. Figure 3-2(A) shows only minor features in the sample recrystallized with a 1 μm sputtered oxide cap: the flatness of this film is truly exceptional. The sample shown in Fig. 3-2(A) was secco etched to delineate grain boundaries; the result is shown in Figure 3-3 and it indicates that rather large grain silicon films can result after laser recrystallization. Grain sizes of 5 x 20 μm are typical.

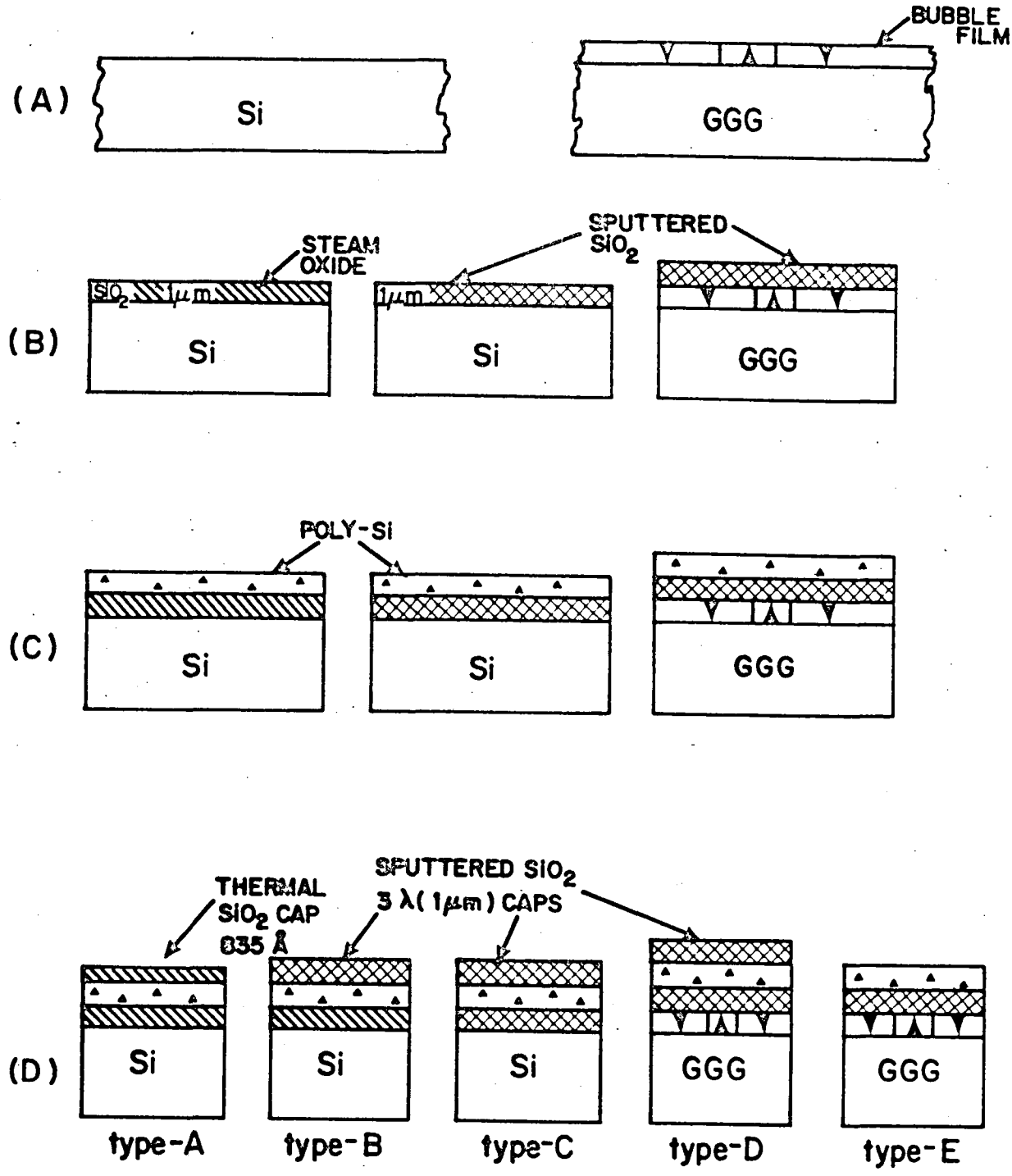
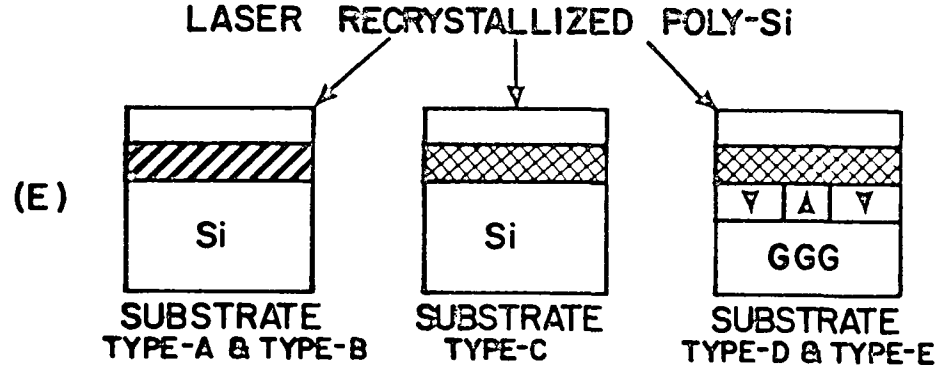
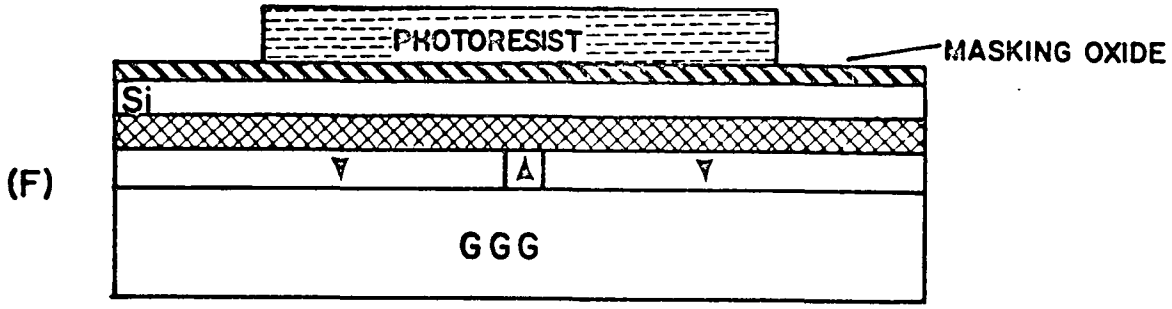
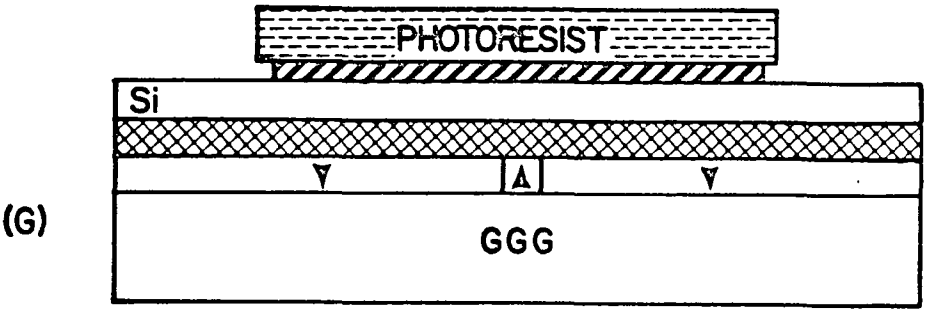
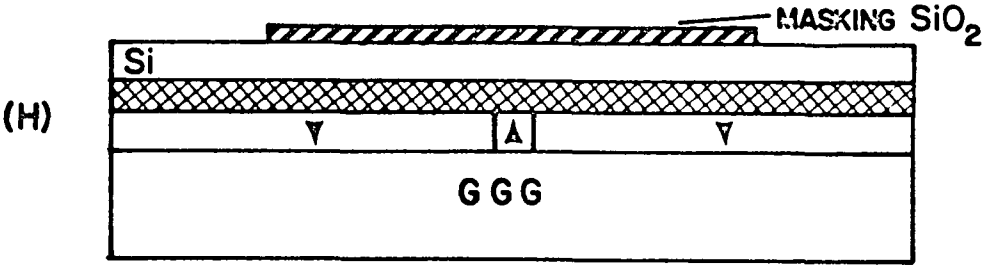


Figure 3-1: Silicon on garnet process flow. (A)-(E) show the process variation studied in this thesis. (F)-(M) show processing common to all substrate types.









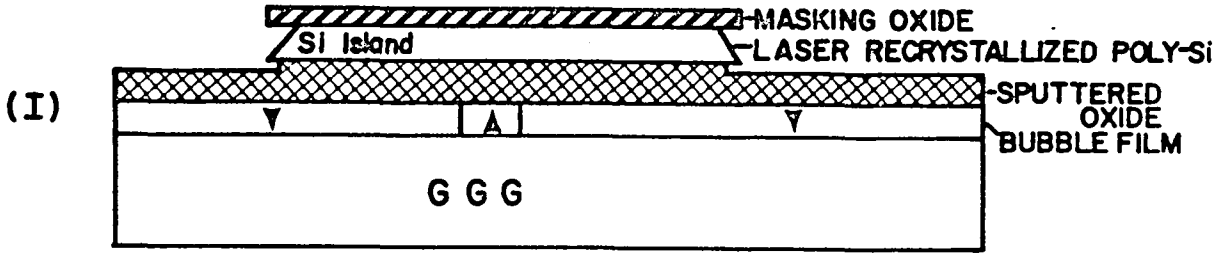
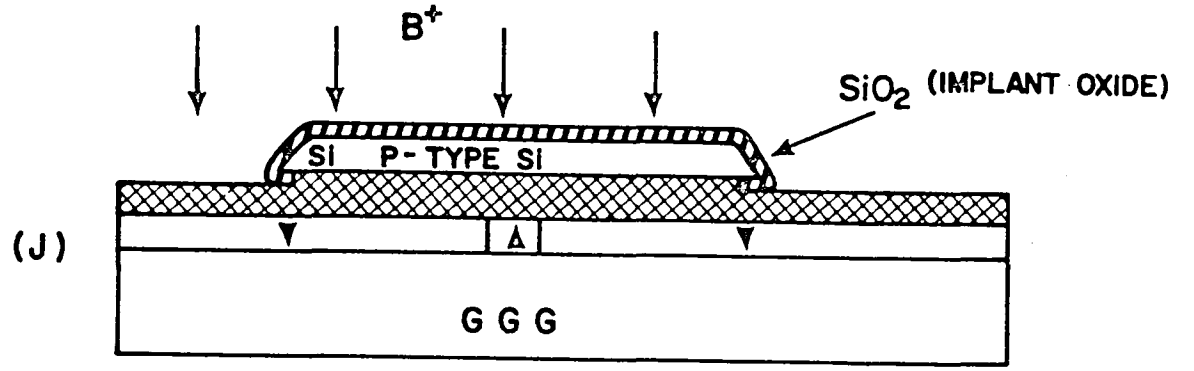
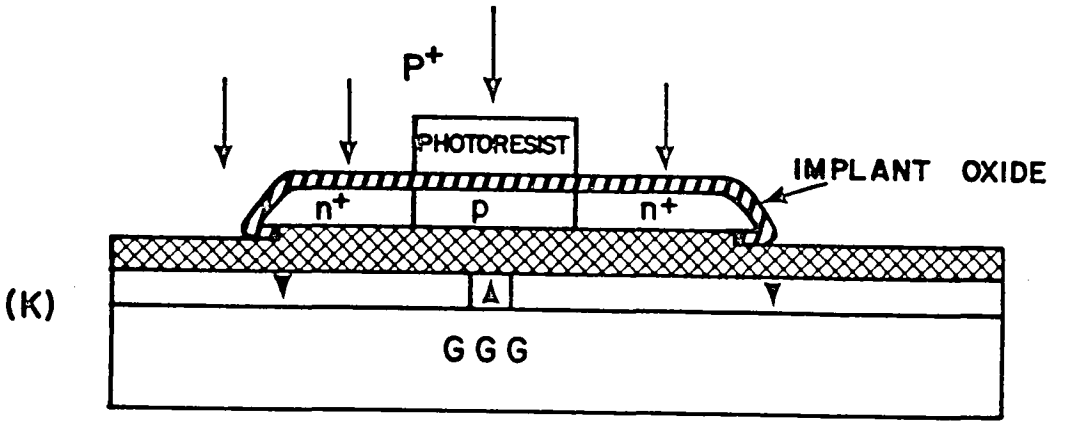
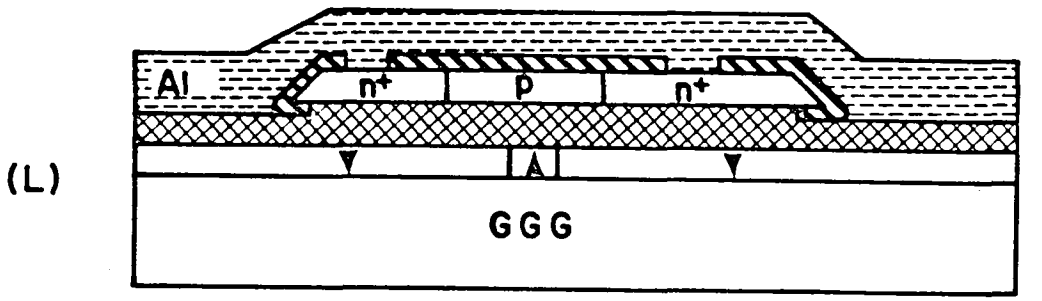


Fig. 3-1 Continued







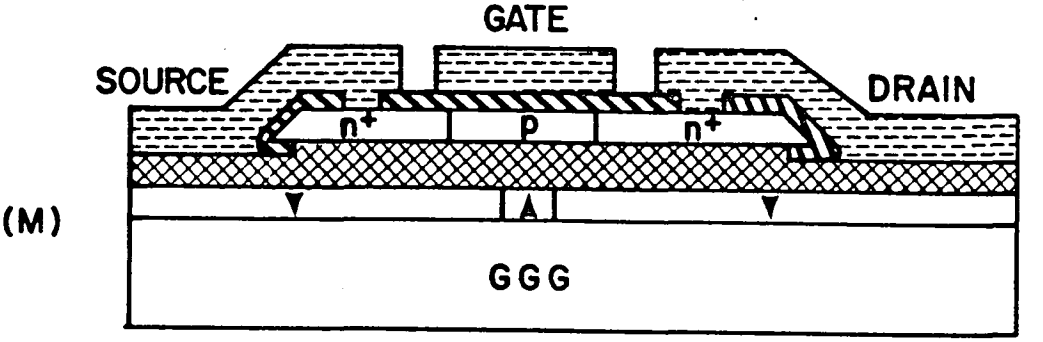


Fig. 3-1 Continued

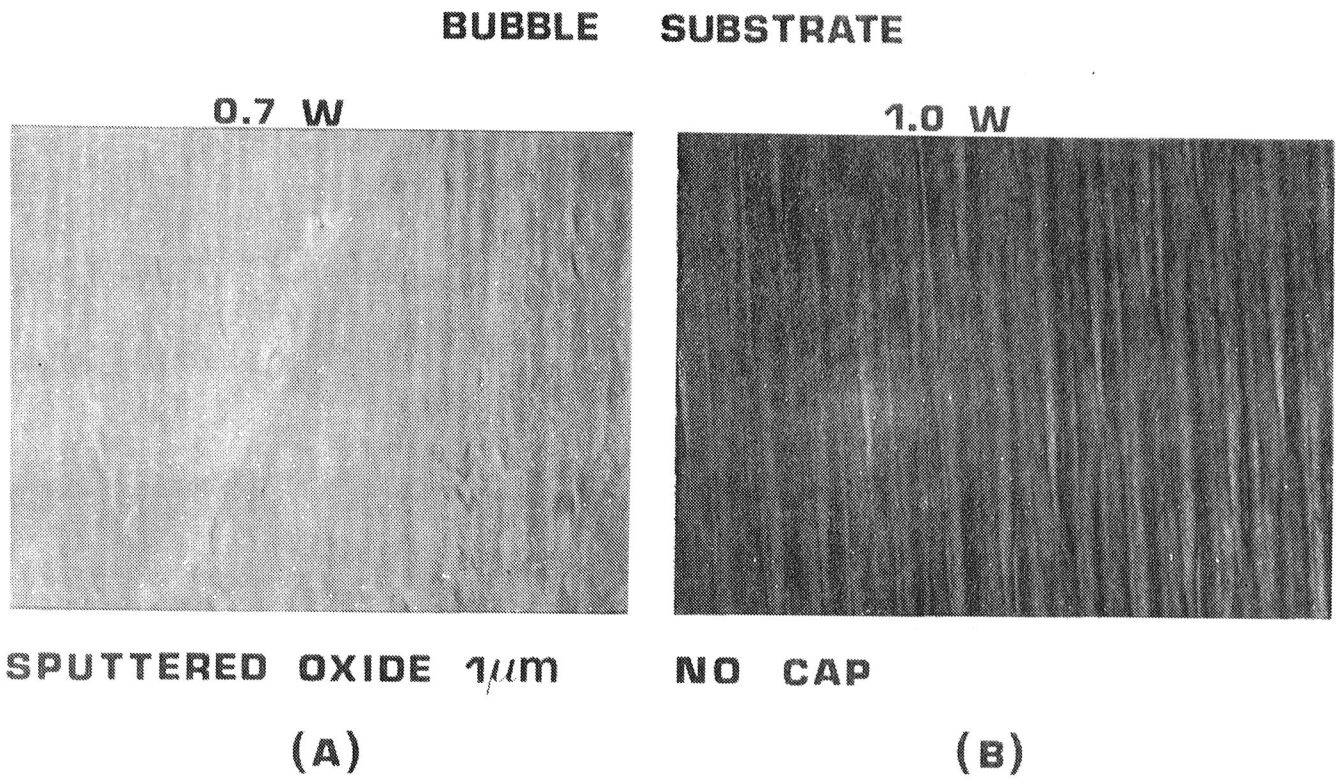


Figure 3-2: Surface texture of recrystallized Si films as a function of cap material, laser power, and substrate type.

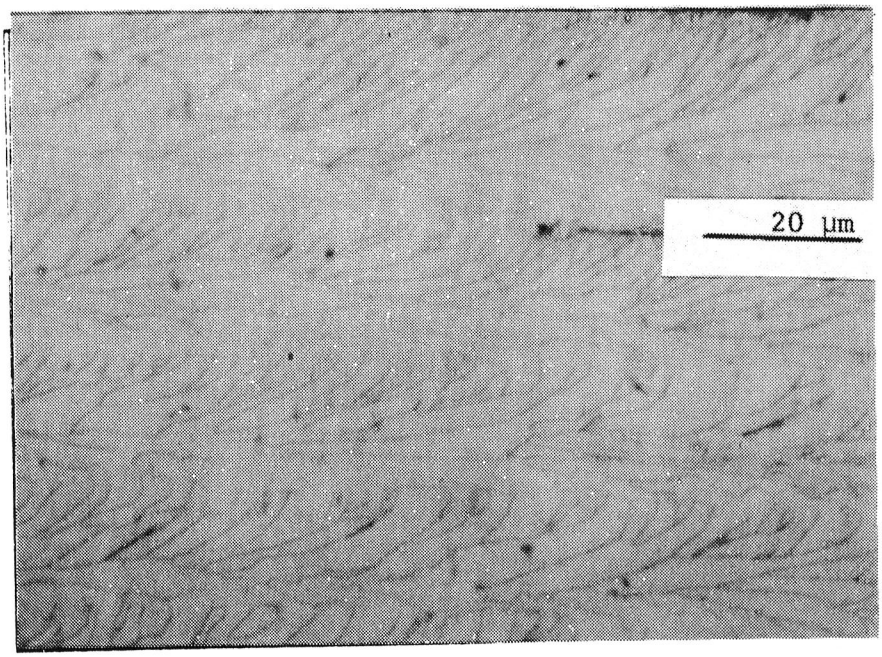


Figure 3-3: Sample of Fig. 3-2(A) after being secco etched.

Films recrystallized on sputtered SiO_2 spacer layers were found to have unwanted features. Figure 3-4 shows a SEM micrograph of a contact window with its aluminum interconnect removed; note the pitting of the recrystallized silicon film. The pitting occurs inside the window (the exposed silicon) and outside of the window (thermal SiO_2 on silicon); this indicates that the composite 415°C/450°C aluminum sinter which preceded this micrograph did not produce the pitting. If it had, the pitting should have been restricted to only the exposed silicon window. Figure 3-5 shows a low magnification view of the device shown in Figure 3-4 with the aluminum interconnect still in place.

3.4. CAPPING EFFECTS

In Section 3.3 it was stated that capping layers affect the flatness of recrystallized films; the effects of capping layers on electronic devices, such as MOSFETs, resistors, etc., is equally important. For this reason, we fabricated MOSFETs on substrate types A and B (Fig. 3-1(D)) using the process described in Section 3.2. Table 3-1 summarizes the important electrical properties of MOSFETs fabricated in material recrystallized with 1 μm sputtered oxide caps and 835 Å thermal oxide caps. I_D^{leak} was measured at $V_{GS} < V_T$ and V_{DS}=5 V; I_G^{leak} was measured at V_{GS}=3 V and V_{DS}=0 V. The gate oxide was grown at 900° C using steam, the channel length to-width ratio (L/W)

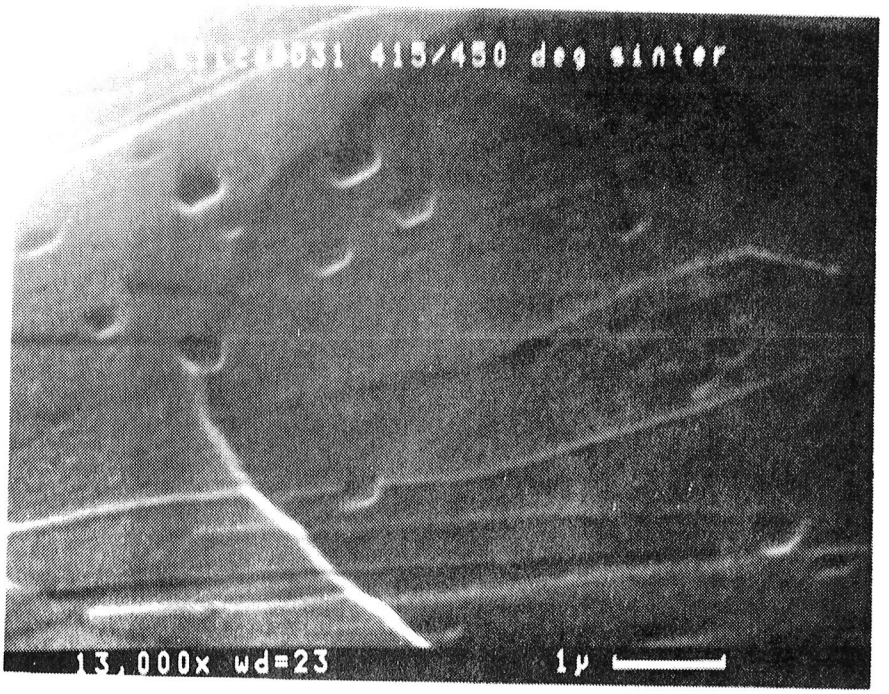


Figure 3-4: SEM micrograph of a contact window with aluminum interconnect removed (wafer D31).

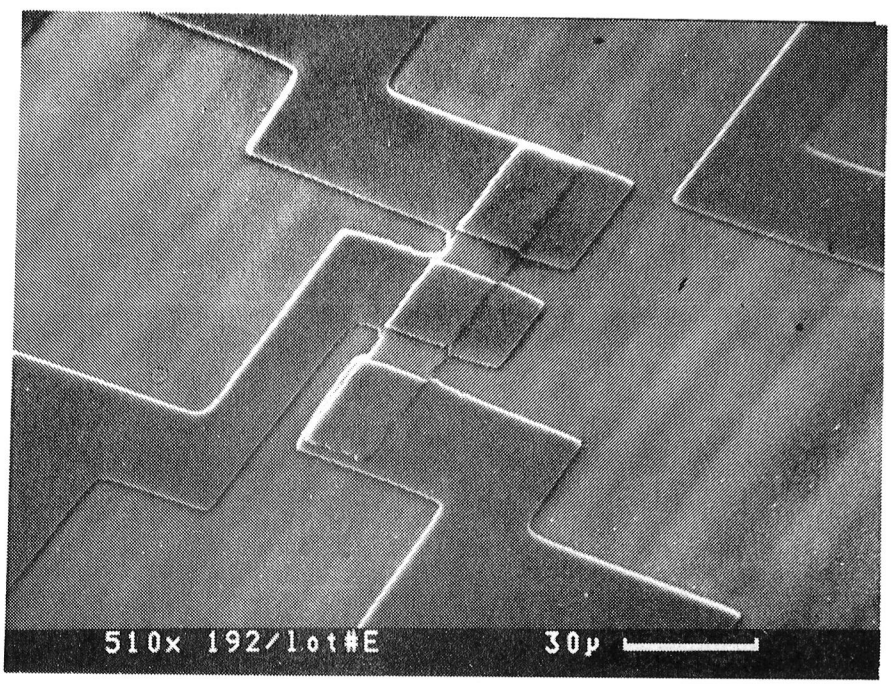


Figure 3-5: SEM micrograph of a silicon on garnet MOSFET (wafer 192)

for these devices was one (L=25μm), and the devices were sintered in nitrogen at 415°C. Additional process details are given in Appendix B.2. The data in Table 3-1

clearly show that a sputtered oxide cap is just as good as a dry thermal oxide cap. Apparently, the sputtered oxide does not contaminate the silicon film during laser recrystallization. This is an important, but surprising, result since the sputtered SiO_2 cannot be as pure as thermally grown SiO_2.

	Sputtered Oxide Cap Wafer ID = D4	Thermal Oxide Cap Wafer ID = D10
$\mu_n = \frac{cm^2}{V\text{-}S}$	306 ± 36	278 ± 29
V_T, Volts	-1.24 ± 0.19	-1.14 ± 0.44
$\mathcal{L}og\ I_D^{leak}$ $[I_D] = A$	-5.92 ± 0.46	-5.96 ± 0.49
$\mathcal{L}og\ I_G^{leak}$ $[I_G] = A$	-10.97 ± 0.30	-10.78 ± 0.10

Table 3-1: The effects of capping layers on MOSFET device parameters (wafers D4 and D10). I_D^{leak} was measured at $V_{GS} < V_T$ and V_{DS}=5 V; I_G^{leak} was measured at V_{GS}=3 V and V_{DS}=0 V.

To determine how pitting of the recrystallized Si layer affects device characteristics, we fabricated MOSFETs on substrate type-C (Fig. 3-1(D)) using the process described in Section 3.2. It was found that the surface morphology of the recrystallized silicon layer plays a role in determining μ_n and V_T. Table 3-2 lists μ_n and V_T for wafers D29 and D30; D29 has only a minor amount of surface pitting while D30 is severely pitted. Note that the threshold voltage for D30 is two times greater than the threshold voltage for D29. Also note that the electron mobility for D30 is three times smaller than it is for D29. Wafers D29 and D30 were fabricated using the same process and at present we can't explain why one wafer is more severely pitted than the other. Random fluctuations in laser power and/or scan speed during recrystallization might be responsible for the different pit densities. It is also possible

that density fluctuations in the sputtered SiO_2 layers could lead to pit formation during recrystallization. In this case, the laser anneal would collapse any voids present in the sputtered oxide layers, thereby densifying the layers. This densification would produce uneven sputtered SiO_2 interfaces to which the molten Si could conform to.

	Wafer ID = D29	Wafer ID = D30
μ_n, $\frac{cm^2}{V\text{-}S}$	22 ± 12	7.0 ± 3.5
V_T, Volts	2.1 ± 0.5	4.2 ± 0.3
$\frac{L}{W} = 1$ for all devices measured.		

Table 3-2: Field effect electron mobility and threshold voltage as a function of surface pit density (wafers D29 and D30)

3.5. ANOMALOUS MOSFET CHARACTERISTICS

We often found that our devices exhibited anomalous behavior. The previous section describes one such case; Section 3.4 shows that pitting of the recrystallized silicon film adversely affects the field effect mobility and threshold voltage of silicon MOSFETs. Before more results are presented, we will describe what can go wrong with MOSFETs and relate these departures from ideality to device characteristics. This divagation will prove to be quite useful in subsequent sections.

First, consider the situation in which the metal–semiconductor contacts (Fig. 3-1(M)) are non-ohmic or rectifying. The contacts will be rectifying if a potential barrier exists between the metal and the semiconductor. To simplify the problem at hand, consider an isolated non-ohmic metal–semiconductor contact such as the one shown in Fig. 3-6(A). For forward bias, the contact can be modeled as a battery V_f in series with a forward resistance R_f, where V_f is the cut in potential of the contact (Fig. 3-6(B)). A similar model can be defined for reverse bias, but the battery V_R and the resistance R_R will be different. Figure 3-6(C) shows the I–V characteristic that will

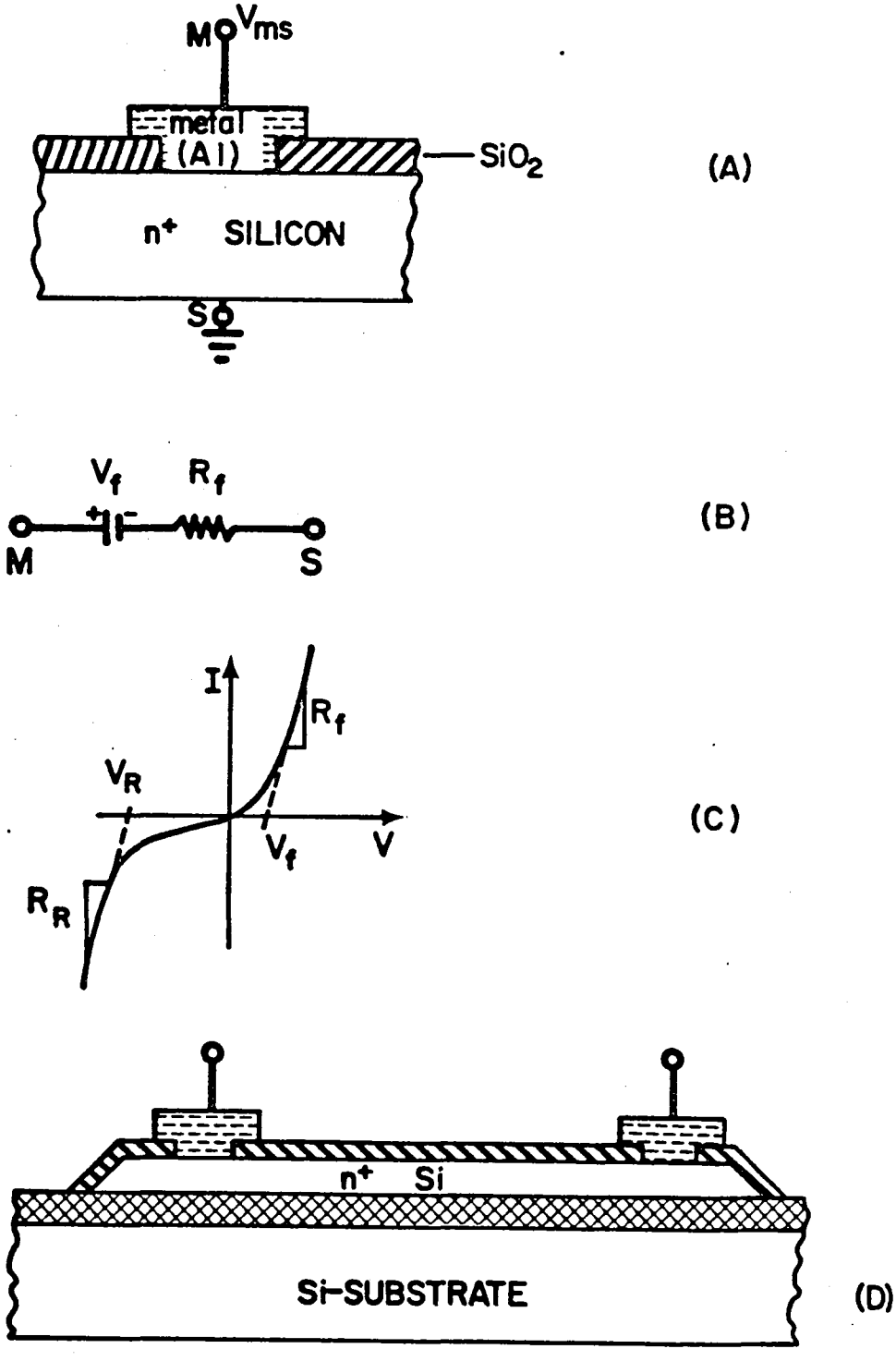


Figure 3-6: (A) Single non-ohmic metal-semiconductor contact. (B) Model of (A) under forward bias. (C) I-V characteristic of (A). (D) Series opposing connection of two non-ohmic metal-semiconductor contacts. (E) I-V characteristic of (D). (F) Physical realization of (D).

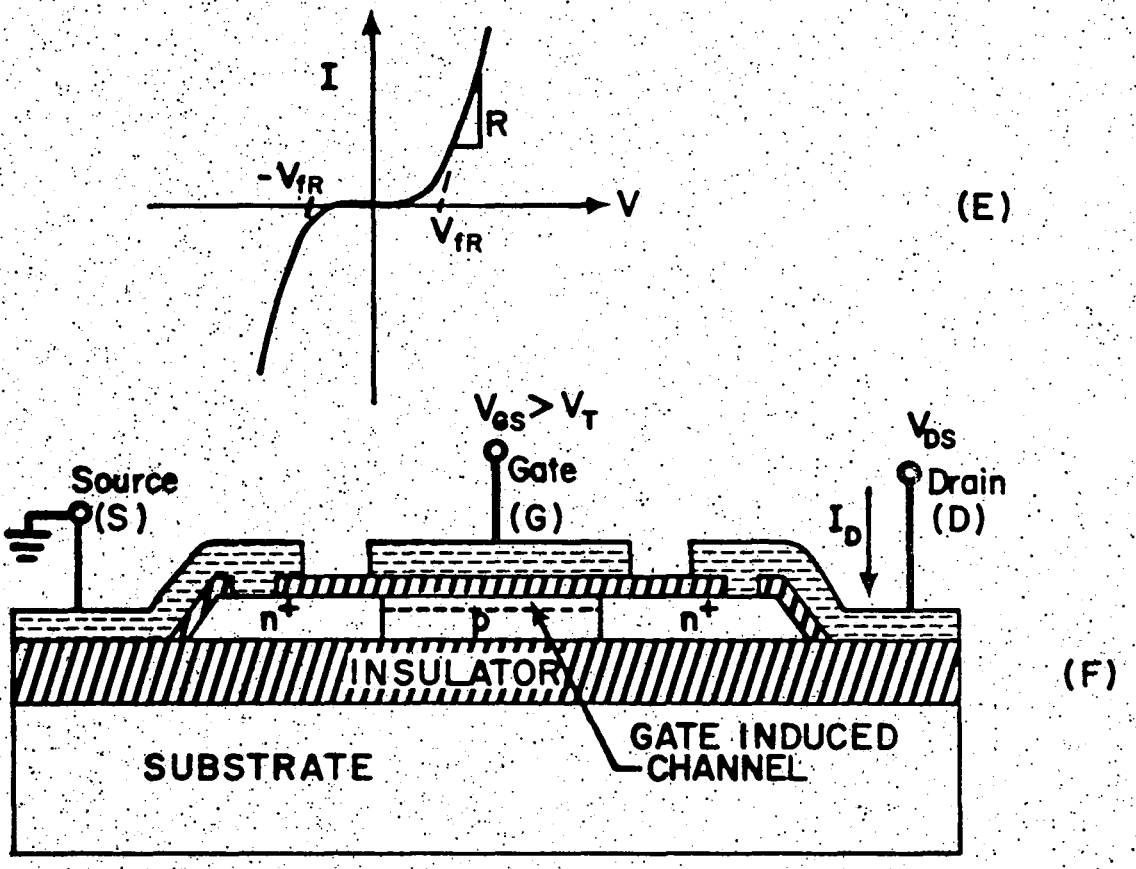


Fig. 3-6 Continued

result for a single non-ohmic metal-semiconductor contact. The forward current results from barrier height lowering and the reverse current results from tunneling.

Consider two contacts in series (Fig. 3-6(D)). This should be a resistor if the contacts were ideal. With non-ohmic contacts, one is always forward biased and one is always reverse biased. Hence, the overall I-V characteristic for the series combination of contacts will be symmetric; Figure 3-6(E) shows this. Now consider a MOSFET with $V_{GS} > V_T$ (Fig. 3-6(F)). This case is analogous to that of the n-type resistor just discussed; however, no drain current I_D is observed until V_{DS} is greater than V_{fR}. Consequently, the I_D vs. V_{DS} characteristic will appear as shown in Fig. 3-7; note the region near the origin where $I_D \simeq 0$.

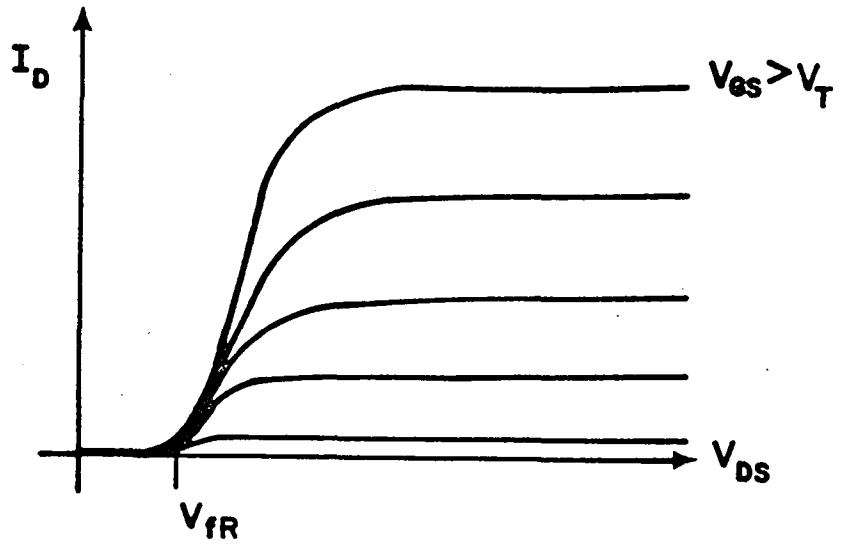


Figure 3-7: Drain characteristics for a MOSFET with non-ohmic contacts.

Figure 3-8 shows our model for a MOSFET with non-zero gate leakage current; currents into the terminals are defined to be positive. R_{ox} is the resistance of the gate oxide, and it may vary with voltage. R_S is a resistor which represents the resistance of the source metal/semiconductor contact, the n^+ source region, and part of the field induced inversion channel. Likewise, R_D is a resistor which represents the resistance of the drain metal/semiconductor contact, the n^+ drain region, and part of the field induced inversion channel. In cutoff ($V_{GS} < V_T$), R_S and R_D are infinite. In the linear region ($V_{GS} > V_T$ and $V_{GD} > V_T$) and the saturation region ($V_{GS} > V_T$ and $V_{GD} \leq V_T$), R_S and R_D are small enough so that significant drain current results.

We can now explain why a non-zero gate leakage current affects the MOSFET I_D vs. V_{DS} characteristic. Fig. 3-9 shows an actual I_D vs. V_{DS} characteristic for a device

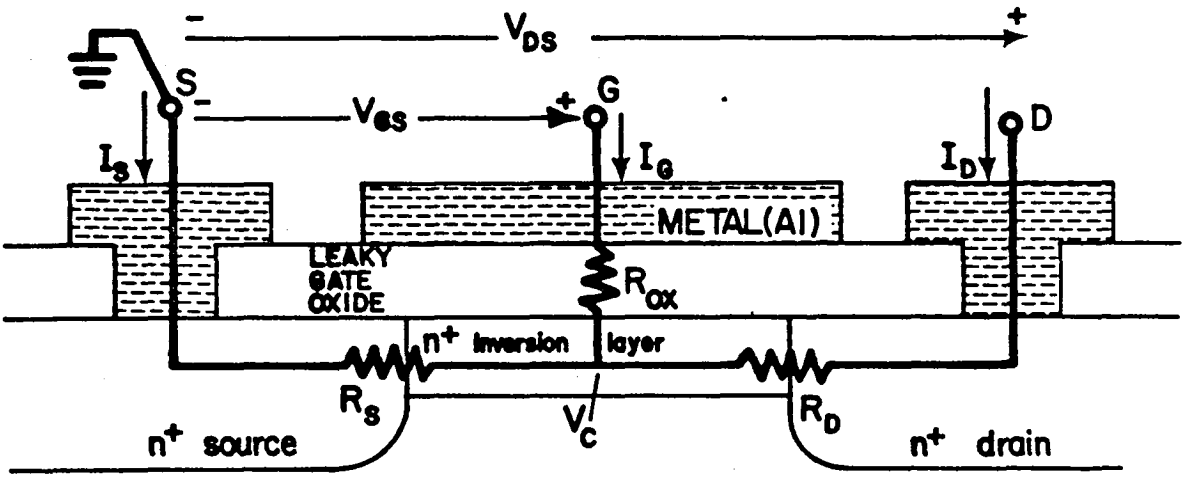


Figure 3-8: Device model for a MOSFET with non-zero, non-catastrophic gate leakage current.

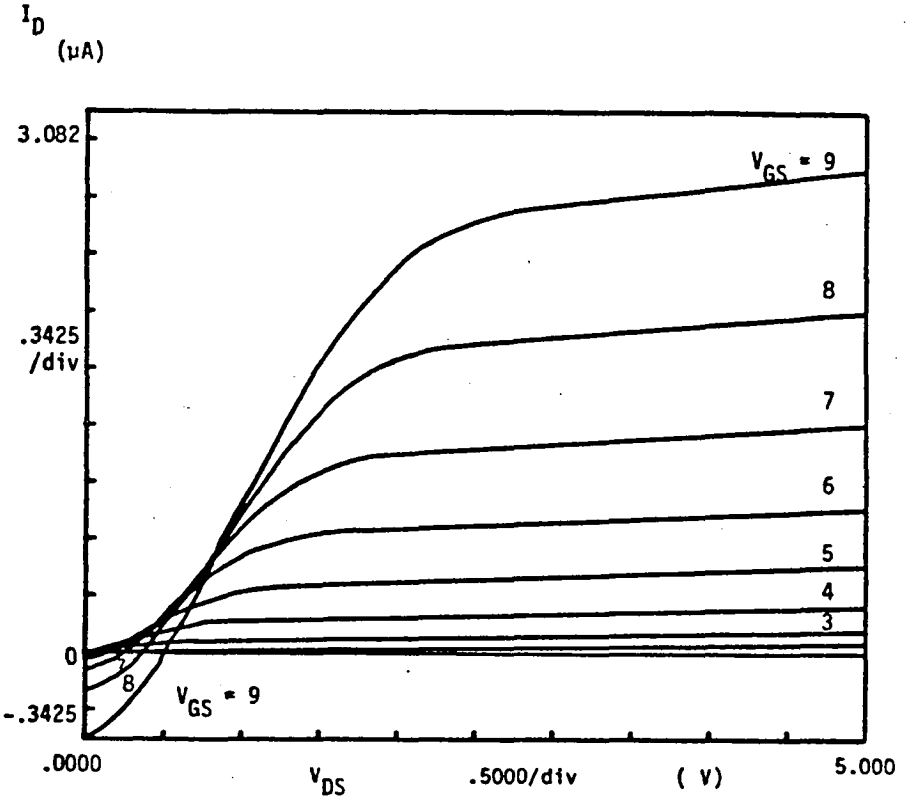


Figure 3-9: Drain characteristics for a MOSFET adequately modeled by the circuit shown in Fig. 3-8 (wafer L10A).

with a leaky gate oxide. For $V_{GS} < V_T$, $I_D = 0$ which is consistent with our model since $V_{GS} < V_T$ implies R_s and $R_D = \infty$. Next consider the case, $V_{DS} = 0$ and $V_{GS} >$

V_T. In this case, $I_G > 0$, and I_S and $I_D < 0$. I_D becomes more negative with increasing V_{GS} (Fig. 3-9). This is also consistent with our model since more voltage is dropped across R_{ox} as V_{GS} increases. Now consider what happens when $V_{DS} \geq 0$ and $V_{GS} \geq V_T$. For this case, I_D is given by

$$I_D = \frac{1}{\theta} V_{DS} + \frac{1}{R_S} \left[1 - \frac{R_D+R_S}{\theta} \right] V_{GS} \qquad \text{Eqn. (3-5)}$$

where

$$\theta \equiv R_D+R_S - \frac{R_S^2}{R_{ox}+R_S} \qquad \text{Eqn. (3-6)}$$

where

$$R_D < \theta < R_D + R_S \quad \text{for} \quad 0 < R_{ox} < \infty. \qquad \text{Eqn. (3-7)}$$

A non-infinite R_{ox} predicts $I_D < 0$ for

$$V_{DS} < \frac{1}{R_S} \left[R_D + R_S - \theta \right] V_{GS} \qquad \text{Eqn. (3-8)}$$

and $I_D > 0$ for

$$V_{DS} > \frac{1}{R_S} \left[R_D + R_S - \theta \right] V_{GS}. \qquad \text{Eqn. (3-9)}$$

Hence, the model thus far fits the data of Fig. 3-9. The point at which I_D changes from negative to positive (i.e. the cross-over point) lies between

$$0 \leq V_{DS} \leq V_{GS} \quad \text{for} \quad \infty > R_{ox} > 0. \qquad \text{Eqn. (3-10)}$$

Note that V_{DS} (cross-over) increases with increasing V_{GS}; again, our model fits the data of Fig. 3-9.

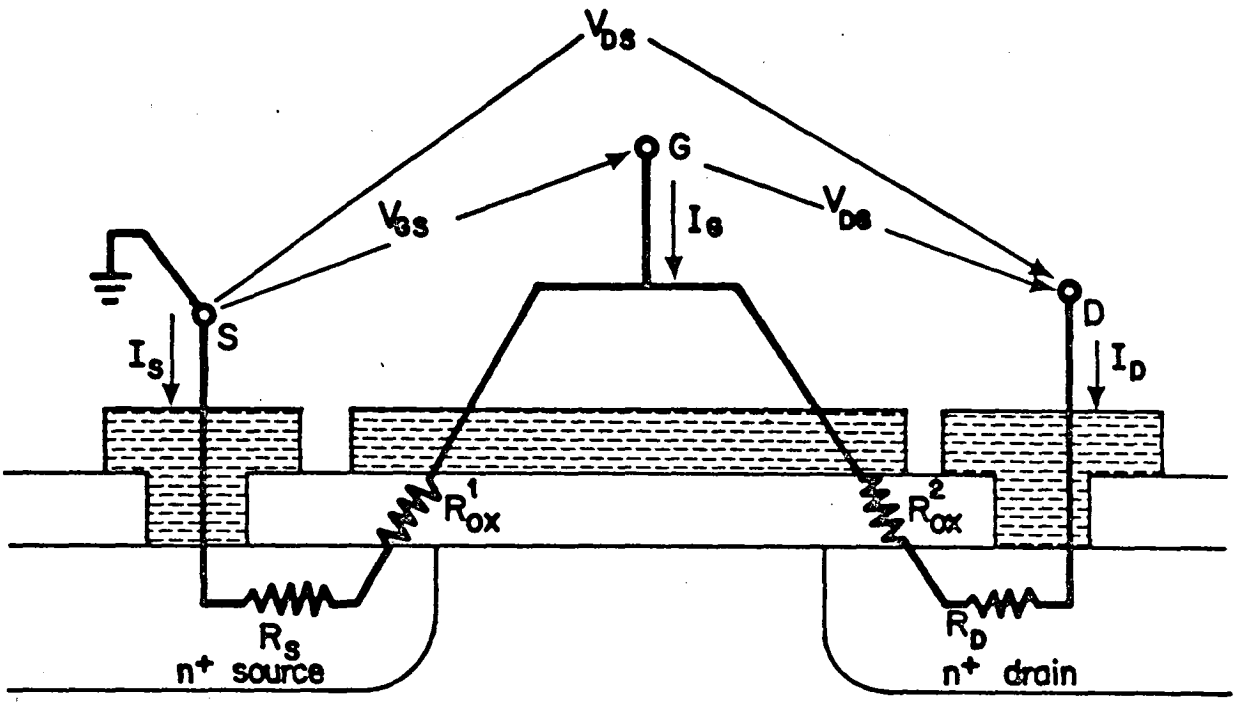


Figure 3-10: Device model for a MOSFET with non-zero, catastrophic gate leakage current.

If the gate leakage current is very large, on the order of a few μA or more, then the model shown in Fig. 3-8 needs to be modified slightly. Figure 3-10 shows the model with the required changes. In essence, the resistance of the gate oxide is so small that an inversion layer cannot be formed. That is, the gate cannot retain enough charge to act as a MOS capacitor. Figure 3-11 shows the type of characteristic which results in such a case. Again, this characteristic is for a fabricated MOSFET. The fact that the I_D vs. V_{DS} curves (often lines, but not always) shift up and down with V_{GS} does not imply that the device is exhibiting the classical-MOSFET field-effect behavior. To see that this is the case, consider each of the three curves. First, take the case of the V_{GS} = -1 V curve. It is clear that $V_{DG} > 0$ for $V_{DS} > 0$. Hence, $I_D > 0$ for $V_{DS} > 0$; furthermore, $I_D = V_{DG}/(R_D+R^2_{ox})$ increases with increasing V_{DS}. Next, consider the V_{GS} = 0 curve. The downward shift of this curve relative to the V_{GS} = -1V curve occurs since V_{DG} is smaller at each V_{DS} for the V_{GS} = 0 case than it is for the V_{GS} = -1 case. Finally, consider the V_{GS} = 1V curve. For $V_{DS} < V_{GS}$ = 1V, it follows that $V_{DG} < 0$ and $I_D < 0$. I_D will tend toward zero since V_{DG} becomes less negative with increasing V_{DS}. When $V_{DS} > V_{GS}$ = 1V, it follows that I_D becomes positive and will increase with increasing V_{DS} since V_{DG} increases with increasing V_{DS}. Note, the $-I_D$ to $+I_D$ cross-over point will occur at higher V_{DS} as V_{GS} is increased.

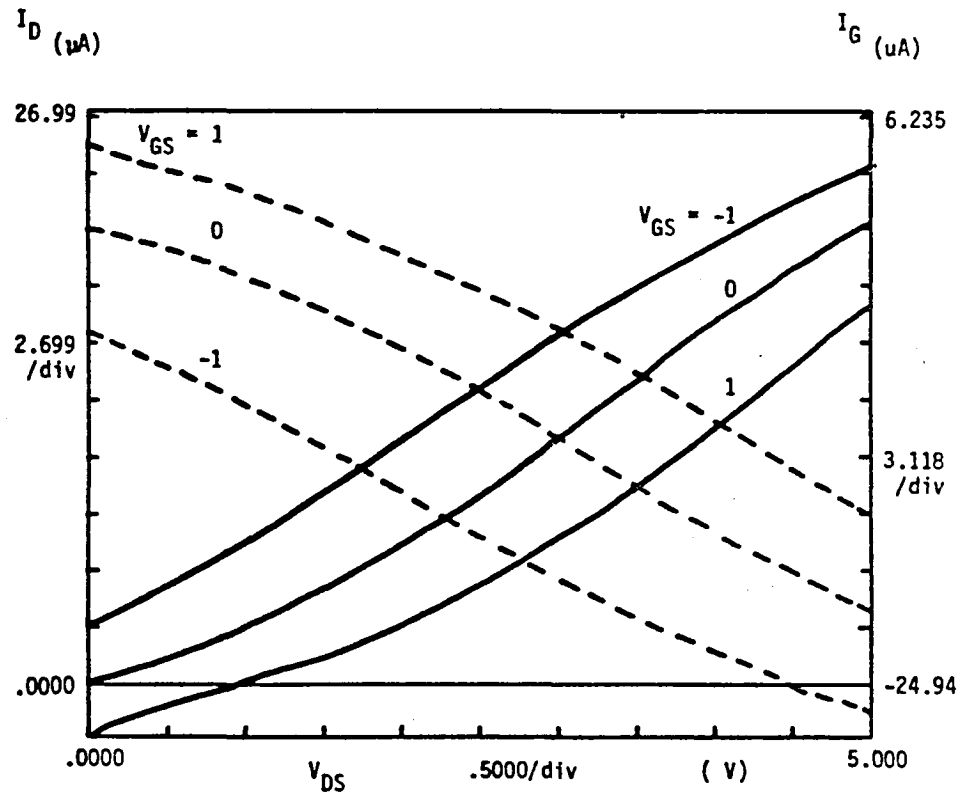


Figure 3-11: Drain characteristics for a MOSFET adequately modeled by the circuit shown in Fig. 3-10 (wafer L10A). Dashed curves are plots of I_G vs. V_{DS}.

3.6. CONTACT RESISTANCE

The effect of contact resistance on MOSFET characteristics was covered in the previous section. In this section, we present results that indicate our metal-semiconductor contacts are non-ohmic. Resistors of n- and p-type were fabricated on substrate types B and C (Fig. 3-1(D)). The process used to fabricate these resistors is essentially the one outlined in Section 3.2; however, the p-type resistors are completely covered by photoresist during the source/drain implant. After fabrication, the cut-in potential V_{TR} and resistance R (Fig. 3-6(E)) were measured. The resistors were then sintered at 415°C in nitrogen for 30 min. V_{TR} and R were measured again following the sinter.

3.6.1. Resistors on Thermal SiO_2 Layers

Table 3-3 lists the before and after sinter values of V_{fR} and R for n- and p-type resistors. This table clearly shows the sinter reduces V_{fR} and R for both n- and p-type resistors. The resistance of the n-type resistor is reduced by a factor 2.25 while the resistance of the p-type resistor is reduced by a factor of 37. Cut-in potentials are also reduced significantly: V_{fR} for n-type resistors is cut in half as a result of the sinter; V_{fR} for p-type resistance is reduced by a factor of 11 after the sinter. The I-V characteristics of n-type resistors were typically symmetric and had shapes similar to the one in Fig. 3-12; however, the I-V characteristics of p-type resistors were sometimes highly asymmetric. At present we cannot explain the origin of this asymmetry. But we have found, a post-metallization sinter can introduce symmetry to the I-V characteristics of some p-type resistors.

	Wafer ID = D3			
	n-Type Resistor		p-Type Resistor	
	R	V_{fR}	R	V_{fR}
Before Sinter	46.8 ± 14.8 kΩ	1.71 ± 0.20	150 ± 82 MΩ	4.89 ± 0.36
After 415°C 30 min. N_2 Sinter	20.4 ± 2.9 kΩ	0.85 ± 0.07 V	4.2 ± 2.3 MΩ	0.44 ± 0.96

Table 3-3: Resistance and cutin potential for n- and p-type resistors on thermal oxide spacer layers, before and after sinter (wafer D3).

Mobility values for the n- and p-type resistors may be calculated. The linearity of our resistor characteristics over large voltage ranges (20 - 100 V is common) indicates that the properties of laser recrystallized polysilicon can be taken to be essentially those of single crystal silicon. Therefore, the conductivity of such a layer is given by

$$\sigma = n\mu_{n,p}q = \frac{N\mu_{n,p}q}{t} \qquad \text{Eqn. (3-11)}$$

where N is the implanted dose of n- and p-type impurities, and t is the thickness of the doped layer which can be less than the thickness of the recrystallized Si film. The resistor's value is given by

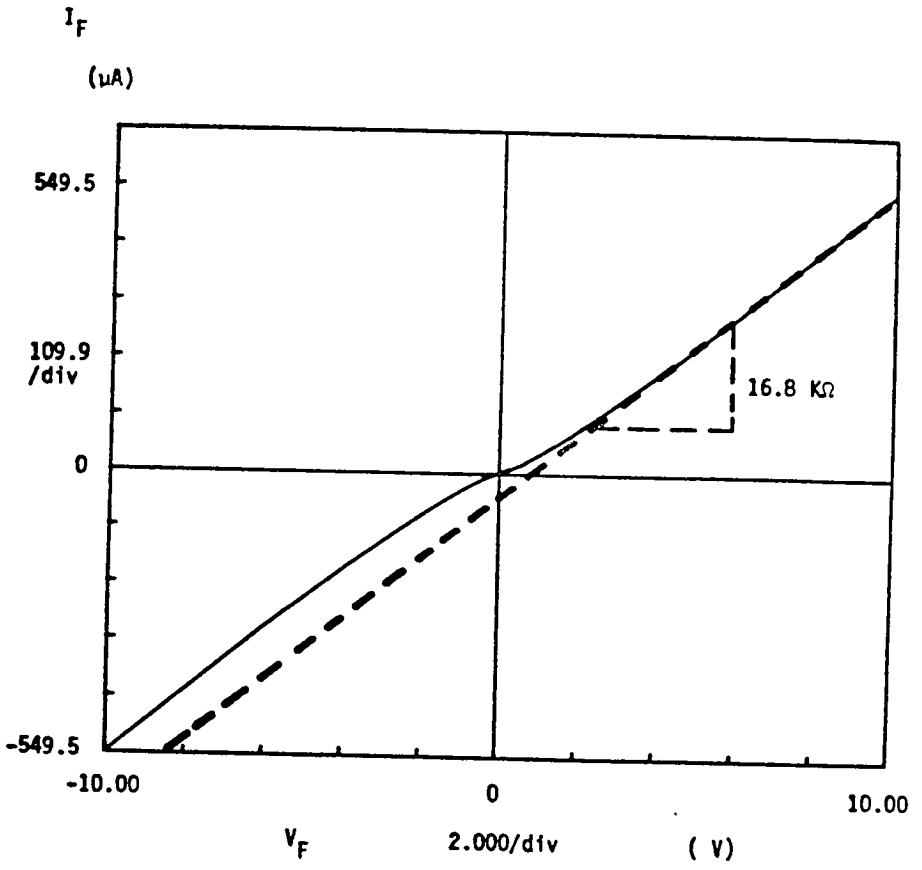


Figure 3-12: I-V characteristic for an n-type resistor after a 30 min. nitrogen sinter (wafer D3).

$$R = \frac{\ell}{\sigma W t} \qquad \text{Eqn. (3-12)}$$

where ℓ is the length of the resistor, and W is its width. Using Eqn. (3-11) in Eqn. (3-12) gives

$$\mu_{n,p} = \frac{\ell}{N\ R\ qW}. \qquad \text{Eqn. (3-13)}$$

From Eqn. (3-13), Table 3-3, and Table 3-4, we calculate μ_n = 92 $cm^2/V\text{-}S$ and μ_p = 223 $cm^2/V\text{-}S$. The higher mobility for holes follows since $\mu_p > \mu_n$ for the doping levels used in our devices ($\sim 2 \times 10^{18}$ for n-type resistors and $\sim 2 \times 10^{15}$ for p-type resistors).

For All Wafers	
n-Type Resistor	p-Type Resistor
ℓ = 600 μm W = 20 μm N = 1 x 10^{14} cm^{-2} t = 0.5 x 10^{-4} cm	ℓ = 300 μm W = 20 μm N = 1 x 10^{11} cm^{-2} t = 0.5 x 10^{-4} cm

Table 3-4: Geometrical parameters for n- and p-type resistors.

3.6.2. Resistors on Sputtered SiO_2 Layers

Table 3-5 lists the before and after sinter values of V_{fR} and R for n-type resistors. This table shows that the sinter reduces R and increases V_{fR}. The resistance is reduced by a factor of 1.45 and V_{fR} is quadrupled. One would expect that the sinter would, if anything, lower V_{fR}, not raise it. At present we do not understand the sinter induced increase in V_{fR}. We speculate that the increase has something to do with a gross contamination of the Si layer by the sputtered oxide spacer layer.

Equation (3-13) can be used to calculate the bulk mobility μ_n since R, ℓ, N, q, and W are known quantities; therefore, μ_n = 10.7 $cm^2/V\text{-}S$. Of course, this calculation is based on the approximation that the properties of laser recrystallized Si are reasonably close to those of single crystal Si (same approximation as was made in Section 3.6.1). The electron mobility for n-type silicon on sputtered SiO_2 is 8.6 times smaller than it is for n-type silicon on thermally grown SiO_2. We attribute the lower μ_n for sputtered SiO_2 spacer layers to contamination inherent in these layers. The contaminating ions may introduce trap levels within the silicon bandgap; thereby reducing the electron mobility compared to the contamination free case. Moreover, the contaminating ions may act as scattering centers, further lowering μ_n.

	Wafer ID = D29	
	n-Type Resistor	
	R	V_{fR}
Before Sinter	254 ± 30 KΩ	0.69 ± 0.07 V
After 415°C 30 min. N_2 Sinter	175 ± 21 KΩ	2.84 ± 0.58 V

Table 3-5: Resistance and cutin potential for n-type resistors on sputtered oxide, before and after sinter (wafer D29).

3.7. SPUTTERED VS. THERMAL SiO_2 SPACER LAYERS

It has been shown that μ_n (bulk) is smaller for devices fabricated on sputtered oxide than it is for devices fabricated on thermal oxide (Section 3.6). This section compares the device parameters of MOSFETs fabricated on substrate types B and C using the process shown in Fig. 3-1. The gate oxide for wafer D4 (thermal oxide spacer layer) was grown at 900°C, and the gate oxide for wafer D29 (sputtered oxide spacer layer) was grown at 850°C; both oxidations were conducted in a steam ambient. All devices underwent a 30 min. 415°C N_2 sinter following metalization. Additional process details are given in Appendix B. It should be noted that both devices had identical geometries; the length to width ratio L/W was one (L=25μm). In addition, I_D^{leak} was measured at $V_{GS} < V_T$ and V_{DS}=5 V; I_G^{leak} was measured at V_{GS}=3 V and V_{DS}=0 V.

Devices fabricated on sputtered oxide spacer layers have surface mobilities which are nearly 10 times smaller than those fabricated on thermally grown SiO_2 spacer layers. In addition, it was found that devices fabricated on sputtered oxide have larger gate leakage currents than those fabricated on thermal oxides; the difference is typically 5 orders of magnitude. Such a gross difference indicates significant contamination of the gate oxide. This contamination most likely results from diffusion of impurities from the sputtered SiO_2 to the recrystallized silicon layer. This diffusion must take place after the laser recrystallization since Section 3.4 has shown that sputtered SiO_2 caps do not have an adverse effect on MOSFET performance. It was also found that devices fabricated on sputtered oxide had lower gate oxide breakdown voltages compared to devices fabricated on thermal oxide. The gate oxide breakdown field for MOSFETs on

wafer D29 was ~ 0.5 - 0.6 x 10^6 V/cm; for reference, a high quality gate oxide has a breakdown field strength of 6 x 10^6 V/cm or greater. In conclusion, Table 3-6 lists the electrical properties of MOSFETs with sputtered and thermal SiO_2 spacer layers.

	Sputtered SiO_2 Spacer Layer Wafer ID = D29	Thermal SiO_2 Spacer Layer Wafer ID = D4
μ_n, $\frac{cm^2}{V\text{-}S}$	42 ± 11	306 ± 36
V_T , Volts	-0.25 ± 0.64	-1.24 ± 0.19
$\ell og\ I_D^{leak}$ I_D in amps	-6.13 ± 0.38	-5.92 ± 0.46
$\ell og\ I_G^{leak}$ I_G in amps	-5.57 ± 2.0	-10.97 ± 0.30

Table 3-6: The effects of thermal and sputtered oxide spacer layers on MOSFET device parameters (wafers D4 and D29). I_D^{leak} was measured at $V_{GS} < V_T$ and V_{DS}=5 V; I_G^{leak} was measured at V_{GS}=3 V and V_{DS}=0 V.

3.8. MOSFETS ON BUBBLE SUBSTRATES

The single most important accomplishment of this work is the fabrication of working MOSFETs on magnetic bubble substrates (substrate type-D Fig. 3-1(D)). Figure 3-13 shows the I_D vs. V_{DS} characteristic for one of our better devices. The classic field effect characteristic is clearly evident; this MOSFET is fabricated on a LPE bubble film (LPE film is supported by a GGG substrate) whose composition is $(Y_{1.00}Sm_{0.39}Tm_{0.92}Ca_{0.69})(Ge_{0.70}Fe_{4.30})O_{12}$. The process used to fabricate this MOSFET is the same one discussed in Section 3.2; it should be also noted that the devices did not undergo a sinter following the metalization. The crossover of the V_{GS} = 8 and 7 V curves is indicative of a gate leakage current problem. Figure 3-9 shows a similar characteristic; the cross-over phenomena is more readily apparent in this figure. The

flat portion of the I_D vs. V_{DS} characteristic near the origin in Fig. 3-13 is indicative of rectifying metal-semiconductor contacts. Figure 3-14 shows a plot of I_G^{leak} vs. V_{DS} for different gate to source voltages superimposed on the drain characteristics (note the I_G scale is in nA while the I_D scale is in μA). The decrease of I_G for increasing V_{DS} at constant V_{GS} is expected since the voltage dropped across the oxide toward the drain becomes smaller as V_{DS} increases. In any event, there is still a significant gate leakage problem which must be explained. Table 3-7 bears this out: I_G^{leak} is $\sim$ 3 orders of magnitude worse for MOSFETs built on bubble substrates coated with sputtered SiO_2 than it is for MOSFETs built on silicon substrates coated with sputtered SiO_2 when we compare non-sintered devices. Again, such a large difference indicates contamination of the gate oxide and the recrystallized silicon layer. We hypothesize that the contamination results from diffusion of ions from the bubble film and sputtered oxide spacer into the recrystallized Si film. Moreover, we suspect that the contaminating ions are incorporated into the gate oxide during its growth.

	Bubble Substrate Sputtered SiO_2 Spacer Wafer ID = L10A	Silicon Substrate Sputtered SiO_2 Spacer Wafer ID = D33
μ_n $\frac{cm^2}{V\text{-}S}$	6 ± 6	9 ± 9
V_T, Volts	2.4 ± 0.9	2.1 ± 1.2
$\log I_D^{leak}$ I_D in amps	-7.2 ± 0.4	-8.3 ± 0.6
$\log I_G^{leak}$ I_G in amps	-5.3 ± 0.5	-8.0 ± 2

NOTE: L10A and D33 were not sintered.

Table 3-7: MOSFET device parameters as a function of substrate type (wafers L10A and D33). I_D^{leak} was measured at $V_{GS} < V_T$ and V_{DS}=5 V; I_G^{leak} was measured at V_{GS}=3 V and V_{DS}=0 V.

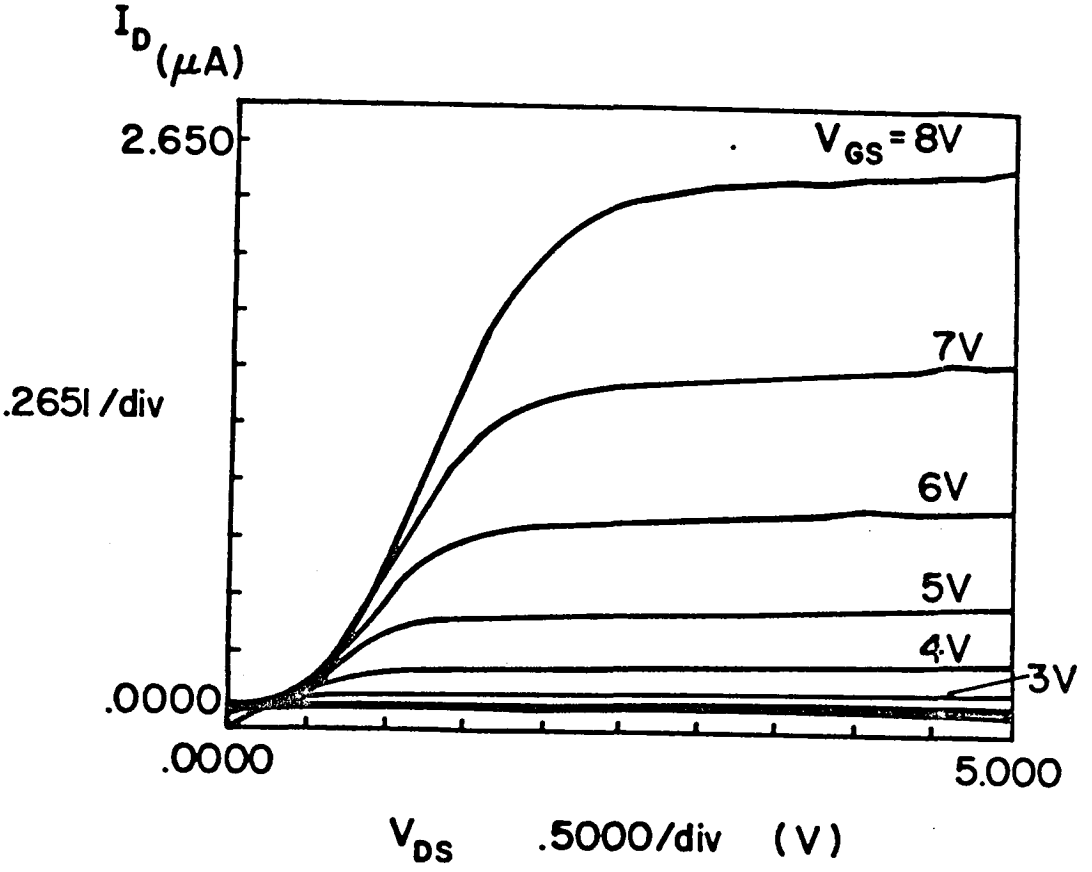


Figure 3-13: Drain characteristics for a silicon on garnet MOSFET (wafer L10A).

The V_T values given in Table 3-7 are most likely artificially high since the devices did not undergo a 30 minute N_2 415°C sinter prior to being probed. This statement was verified experimentally. Wafer D29 was broken into two samples; the first sample was sintered and the second sample was not (MOSFETs in both samples were of similar quality prior to the sinter). The sintered sample produced MOSFETs with V_T = 0.3 ± 0.4 V while the nonsintered sample produced MOSFETs with V_T = 1.9 ± 0.1 V; mobilities of unsintered devices were typically two times smaller than those of sintered devices. The leakage currents, I_D^{leak} and I_G^{leak}, increased by 2-3 orders of magnitude after the sinter. The sinter does not actually cause the increase in $I_{D,G}^{leak}$, but rather it lowers the metal (Al) semiconductor contact resistance and therefore allows more voltage to be dropped across the semiconductor and/or gate oxide. It is this increased voltage drop which is responsible for larger device currents.

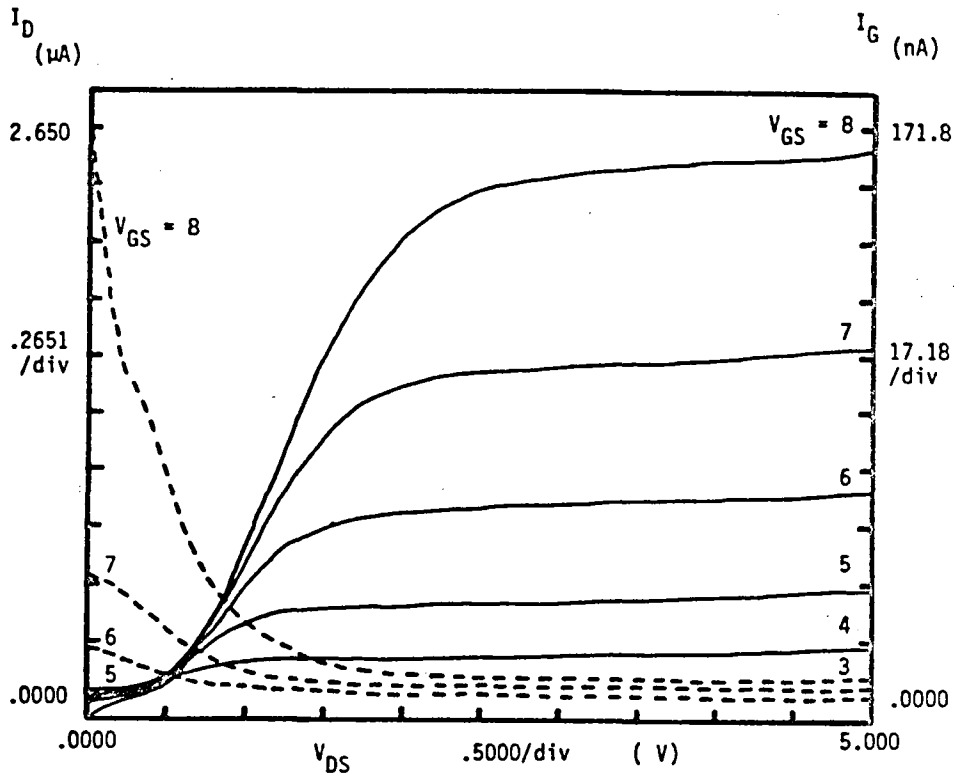


Figure 3-14: I_G^{leak} vs. V_{DS} as a function of V_{GS} (dashed curves) superimposed on the drain characteristics (solid curves) for the device considered in Fig. 3-13

3.9. DISCUSSION

In Section 3.4, it was shown that a severely pitted silicon film has a higher V_T and lower μ_n compared to an unpitted silicon film. These changes in V_T and μ_n are related to the uniformity of the gate-induced electric field. A highly nonuniform electric field will be characteristic of the pitted film; the field will be stronger at the cusps and weaker in the valleys (Fig. 3-15(A)). Consequently, the induced electron concentration will also be nonuniform over the pitted surface: the electron concentration will be greater in the cusps than in valleys. This induced conduction electron concentration gradient is balanced by a potential barrier, ϕ_B, which develops between the cusps and valleys. In fact, Eqn. (1-2) can be used to describe it. These ϕ_B barriers affect μ_n in the same way as additional grain boundaries would; that is, μ_n is reduced as a result of their presence. Furthermore, the electron concentration in the valleys is less than it is for the flat silicon surface (assuming the same gate voltages in both cases). Compare (Fig. 3-15(A) and (B)). This causes V_T to be higher for the pitted surface.

The results presented in this chapter show that working MOSFETs can be fabricated on magnetic bubble substrates; however, these silicon-on-garnet MOSFETs which have thus far been fabricated are far from being ideal. Gate leakage currents are high and electron mobilities are low. In addition to these problems, there are two less serious problems: the first is that MOSFETs fabricated on bubble substrates have high threshold voltages; the second is that the metal-semiconductor contacts are exhibiting significant contact resistances. The high threshold voltages can be reduced by optimizing the laser recrystallization conditions; careful control of the capping and/or spacer layer thickness should result in higher quality recrystallized silicon layers. Thickness variations can drastically change the amount of energy coupled into the silicon film during recrystallization; if the thickness changes by as little as 1/4 λ (1/4 λ = 835 Å, for SiO_2 at 4880 Å), the layer will change from absorbing to reflecting. Most of the films recrystallized in this work had cap or spacer layers which varied in thickness by as much as 1000-4000 Å. This type of thickness variation will greatly affect the grain size of the recrystallized silicon film; in fact, it has been shown experimentally (with a microscope) that silicon regions under some parts of the cap are not recrystallized, while those under other parts of the cap are. Source/drain contact resistance problems can be reduced by doping these regions at higher levels; 10^{19} to $10^{20}cm^{-3}$ will be used in future silicon-on-garnet device lots. In previous lots, the source and drain regions were doped at $\sim 2 \times 10^{18}cm^{-3}$.

Sections 3-7 and 3-8 attribute the observed gate leakage current to gate oxide contamination. At present, the identities of the contaminants are not definitely known. Likely candidates include Fe, Ga, Sm, Gd, Tm, Y; in short, any bubble film ion other than oxygen. It seems likely that static gate current flows through the gate oxide by some type of tunneling phenomenon. Fowler-Nordheim tunneling can be ruled out because the gate to source voltages used in our work are at least an order of magnitude too small to generate an appreciable Fowler-Nordheim current. Trap assisted tunneling, however, is a distinct possibility since some of the contaminants may introduce trap levels within the SiO_2 bandgap. Consider the case in which there is only a single discrete trap level E_T within the SiO_2 bandgap; Figure 3-16(A) shows the energy band diagram for the metal-oxide-semiconductor system when $V_{GS} = 0$ V. Gate current results when $V_{GS} > 0$. The current carriers, electrons in this case, tunnel from the conduction band of the silicon into the unpopulated levels within the oxide bandgap. They next tunnel from traps near the Si-SiO_2 interface to other traps within the oxide; the bias V_{GS} insures that the electrons will tunnel in the direction shown in Fig. 3-

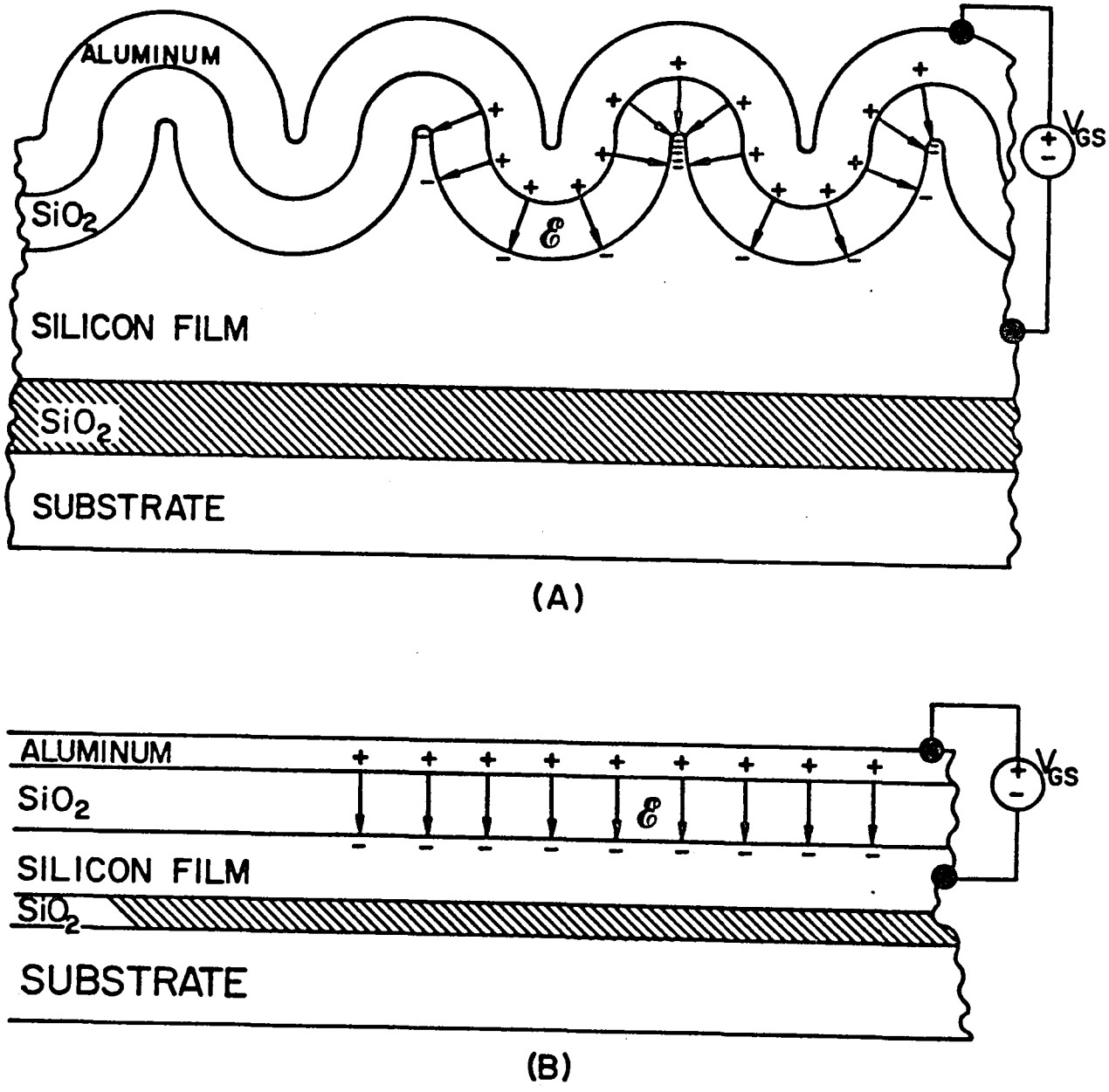


Figure 3-15: (A) Model of a severely pitted silicon surface for $V_{GS} > V_T$.
(B) Model of a flat silicon surface for $V_{GS} > V_T$.

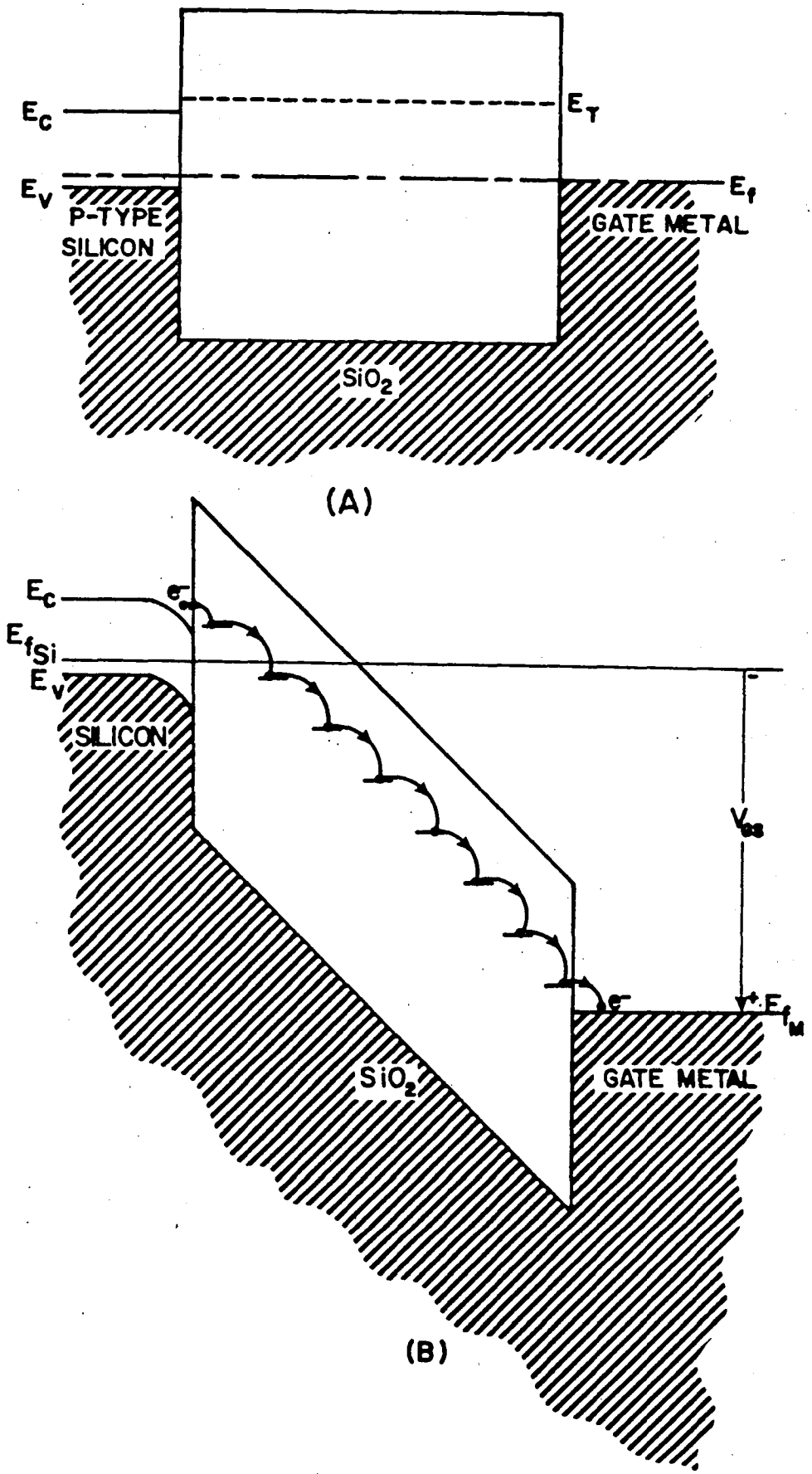


Figure 3-16: (A) Energy band diagram for a MOS system with leaky gate oxide for V_{GS} = 0 V where we have assumed the flat-band voltage is zero. (B) Same diagram as in (A) but under bias.

16(B). Eventually, the electrons reach traps near the SiO_2–metal interface; they next tunnel from these traps to conduction band states in the metal. Still, another possibility results if the contaminants form inclusions. In this case, conduction through the contaminated SiO_2 layer probably proceeds by direct tunneling from one inclusion to the next if they are close enough. However, Poole–Frenkel conduction (field assisted thermal ionization) might also be operative under certain conditions, particularly if the potential wells of the inclusion regions interact with one another (due to their closeness) and significantly lower the energy barriers [38]. At very high levels of contamination, the inclusions may become connected, and in this case the conduction should be controlled by percolation [39, 40].

Contaminated gate oxide layers also imply contaminated silicon layers since gate oxides are not deposited but grown from these layers. In high enough concentrations, the ionic contaminants may act as scattering centers; the net result of such centers is that the carrier mobility decreases. Heavy metals and rare earths may also introduce trap states into the silicon bandgap; these states are consequently in a position to affect V_T as shown in Eqn. (1–1). Threshold voltages for contaminated devices are in fact greater than uncontaminated ones by about 1.0 volts. Grain sizes are comparable for both contaminated and uncontaminated recrystallized silicon layers. In this case, grain size determinations were made visually during device fabrication.

Although the results in this chapter indicate substantial improvement is yet desirable, the successful fabrication of a MOSFET on a bubble substrate is a previously unreported accomplishment and demonstrates the feasibility of this silicon–on–garnet technology. Future work will investigate ways to prevent contamination of the gate oxide and recrystallized silicon layers. We will try to place a diffusion barrier between the silicon and spacer oxide layers; one material being considered for use is Si_3N_4. It may also be necessary to reduce the process temperatures and/or times. In short, we are confident that process optimization will lead to much improved silicon–on–garnet MOSFETs.

APPENDIX A
BUBBLE FILM MEASUREMENTS

$4\pi M_s$ and ℓ values reported in this work were calculated using bubble statics. Fowlis and Copeland give plots of h/ℓ vs. P_o/h and $H_o/4\pi M_s$ vs. P_o/h from which $4\pi M_s$ and ℓ can be found if H_o, P_o, and h are known [30]. These latter 3 parameters of the bubble film can be determined experimentally with little difficulty.

The domain period (twice the zero-field strip width) P_o is measured from a TV monitor or a photograph such as the one shown in Figure A-1. Magnetic domains, such as the ones shown in Fig. A-1, are observed via the Faraday magneto-optic effect [41]. It is important to insure that the magnetic domains are in the lowest energy state before P_o is measured. This can be done by applying a 60 Hz magnetic field perpendicular to the bubble film (an autotransformer and a Helmholtz coil work very well) and gradually reducing its amplitude to zero. Once the domains are in the lowest energy state, the width of a bright or dark strip domain (see Fig. A-1) can be measured; P_o is then twice this width.

Measuring the bubble collapse field (H_o) requires that bubbles be present in the magnetic layer; however, the presence of stripe domains such as those shown in Fig. A-1 in no way implies that bubbles will be present as the perpendicular bias field is increased from zero. In fact, the bubble film could very well be composed of only two domains or domains that are pinned to bubble film defects (such as the circumference of the wafer). One can generate bubbles by momentarily saturating the bubble film in the plane of the film (90° from the preferred orientation of the magnetization vector). It often happens that a bubble lattice is generated as a result of the in plane saturating field. In practice, a simple fast charging RC circuit can be discharged into a solenoid to provide the needed in plane field.

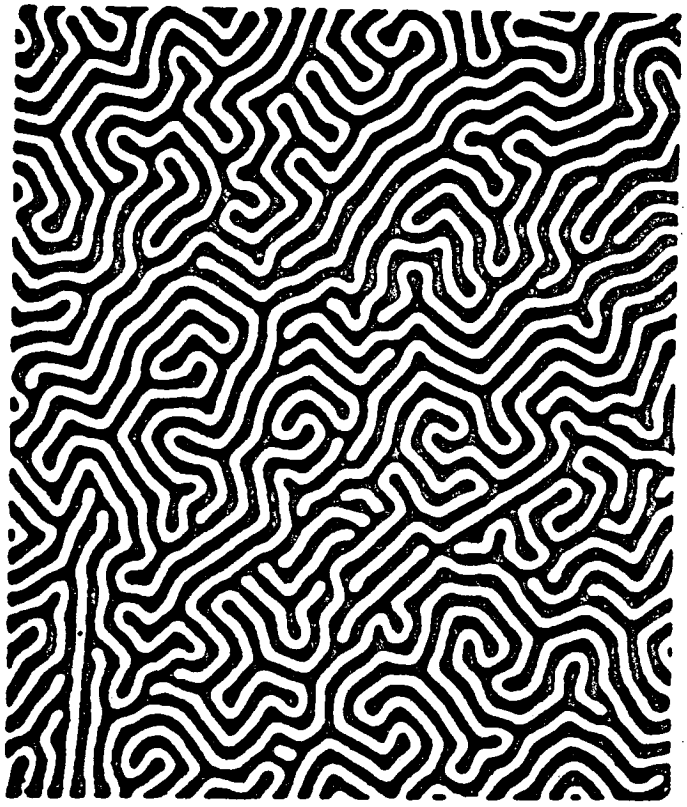


Figure A-1: Magnetic domains observed via the Faraday magneto-optic effect. After Bobeck and Scovil.

Collapse field is the field at which bubbles collapse; however, one must take care to insure that collapse field measurements are only made on isolated bubbles. An isolated bubble is one that is separated from all other bubbles by at least 30-40 ℓ ($\sim$10 bubble diameters). Measurements made on non-isolated bubbles will produce unreproducible results at best since interacting bubbles have collapse fields which are dependent on bubble spacing. In general interacting bubbles also have lower collapse fields.

The thickness (h) of each bubble film is measured using an optical interference technique. Monochromatic light is allowed to impinge upon the bubble film at near normal incidence; the wavelength is then swept monotonically throughout the visible range at a constant rate. Reflected light is detected by a photomultiplier tube and its output is recorded by a chart recorder. The resulting reflectance trace has a significant amount of structure, as might be expected. Film thickness is extracted from the reflectance curve using

$$h = \frac{\frac{1}{2}\Delta N}{\frac{n_1}{\left(\lambda_1^{air}\right)} - \frac{n_2}{\left(\lambda_2^{air}\right)}} \qquad \text{Eqn. (A-1)}$$

where λ_1^{air} and λ_2^{air} are the wavelengths of any two points on the reflectance curve (λ^{air} is the wavelength in air), n_1 and n_2 are the indices of refraction of the bubble film at λ_1^{air} and λ_2^{air}, respectively, and ΔN is the number of cycles between λ_1^{air} and λ_2^{air}. ΔN may be a non-integral value. But in practice, λ_1^{air} and λ_2^{air} are chosen to coincide with the extrema of the reflectance trace for practical reasons. In this case, ΔN = 1/2, 1, 1.5, 2,....

APPENDIX B
SEMICONDUCTOR PROCESS DETAILS

Section 3.2 and Figure 3-1 outline the silicon-on-garnet device fabrication process. In this Appendix we provide additional process details for the interested reader. Section B.1 defines a number of procedures that were used frequently throughout device fabrication; the procedures are referred to as process step units and the reader should refer to them when reading the detailed process descriptions given in Sections B.2 and B.3.

B.1. PROCESS STEP UNITS

PHOTOLITHOGRAPHY

(1) Apply Shipley microposit primer (hexamethyldisilazane (HMDS)).

(2) Spin at 5000 rpm for 30 sec.

(3) Apply Shipley microposit 1350 J positive photoresist.

(4) Spin at 5000 rpm for 30 sec.

(5) 30 min. soft bake at 90°C.

(6) Expose wafer with desired mask level 0.6-0.8 min. at 12 mW intensity.

(7) Develop in Shipley microposit MF-312/CD-27 developer for 1 min. with mild agitation.

(8) Rinse in DI wafer for 2 min. with vigorous agitation.

(9) Blow dry with nitrogen.

(10) 30 min. hard bake at 120°C.

FULL CLEANUP

(1) Place wafers in boiling trichloroethane for 5 min.

(2) Immerse wafers in boiling acetone for 5 min.

(3) Insert wafers in boiling 2-propanol for 5 min.

(4) Rinse in deionized (DI) water for 5 min.

(5) Dip wafers into a solution made up of 3 parts H_2SO_4 and 1 part H_2O_2 for 5 min.

(6) Rinse in DI water for 5 min.

(7) Place wafers in a solution made up of 1 part HF and 10 parts DI water until desired areas are hydrophobic.

(8) Rinse in DI water for 5 min.

(9) Blow dry in nitrogen.

CLEANUP WITH H_2SO_4

(1) Place wafers in boiling trichloroethane for 5 min.

(2) Immerse wafers in boiling acetone for 5 min.

(3) Insert wafers in boiling 2-propanol for 5 min.

(4) Rinse in DI water for 5 min.

(5) Dip wafers into a solution made up of 3 parts H_2SO_4 and 1 part H_2O_2 for 5 min.

(6) Rinse in DI water for 5 min.

(7) Blow dry in nitrogen.

CLEANUP WITH HF

(1) Place wafers in boiling trichloroethane for 5 min.

(2) Immerse wafers in boiling acetone for 5 min.

(3) Insert wafers in boiling 2-propanol for 5 min.

(4) Rinse in DI water for 5 min.

(5) Dip wafers into a solution made up of 1 part HF and 10 parts DI water until desired areas are hydrophobic.

(6) Rinse in DI water for 5 min.

(7) Blow dry in nitrogen.

CLEANUP WITH ORGANIC SOLVENTS

(1) Place wafers in boiling trichloroethane for 5 min.

(2) Immerse wafers in boiling acetone for 5 min.

(3) Insert wafers in boiling 2-propanol for 5 min.

(4) Rinse in DI water for 5 min.

(5) Blow dry in nitrogen.

PHOTORESIST STRIP

(1) Immerse wafers in boiling acetone for 5 min.

(2) Insert wafers in boiling 2-propanol for 5 min.

(3) Rinse in DI water for 5 min.

(4) Blow dry in nitrogen

IMPLANT PHOTORESIST STRIP

(1) Immerse wafers in boiling acetone for 15 min.

(2) Rinse wafers with 2-propanol

(3) Rinse wafers with DI water

(4) Dip wafers in a solution made up of 3 parts H_2SO_4 and 1 part H_2O_2 for 15 min.

(5) Rinse wafers in DI water for 5 min.

(6) Blow dry with nitrogen

SPUTTERED OXIDE DEPOSITION

(1) Pump down to $\sim 1 \times 10^{-6}$ to 5×10^{-7} Torr

(2) Stabilize Ar flow such that Ar pressure is 20 mTorr

(3) 10 min. presputter of SiO_2 target at 700 W.

(4) 60 min. sputter deposition of SiO_2 at 700 W.

(5) 20 min. cool down

(6) Cease Ar flow and vent.

B.2. DETAILED PROCESS DESCRIPTION FOR WAFERS D3, D4, D7, D10

This section lists the process steps that were used to fabricate devices on substrate types A and B (Fig. 3-1(D) and Section 3.2). The gas flow rate for all oxidations, steam and dry, was 1 liter per min. For the steam oxidations, we bubbled pure oxygen through DI water at 95°C and then fed this "wet" oxygen to the furnace tube. One final note, HMDS (an adhesion promoter for photoresist) was not available when wafers D3, D4, D7, and D10 were processed. The wafers were baked at ~200°C for ~30min. prior to all photolithographic steps to promote the adhesion of photoresist. This treatment did not always work; in such cases, we increased the temperature of the dehydration bake (step 23 is an extreme case).

Step Number — Description

(1) Full cleanup (Fig. 3-1(A))

(2) Steam oxidation at 1100°C, 144 min., t_{ox} = 9575 Å (spacer layer Fig. 3-1(B))

(3) Polysilicon deposition at 625°C, 0.75 μm (Fig. 3-1(C))

(4) Full cleanup

(5) Dry oxidation at 1100°C, 27 min., t_{ox} = 835 Å (Antireflection cap for wafers D7 and D10, Fig. 3-1(D)).

(6) Sputtered oxide deposition (3λ antireflection cap for wafers D3 and D4, Fig. 3-1(D))

(7) Laser recrystallization, 4W, substrate temperature = 400°C, scan speed = 20 cm/sec.

(8) Remove antireflection caps in HF (Fig. 3-1(E)).

(9) Rinse in DI water and blow dry with nitrogen.

(10) Steam oxidation at 1100°C, 13 min., t_{ox} = 3000 Å (masking oxide, Fig. 3-1(F))

(11) Photolithography first mask, (silicon island definition level, Fig. 3-1(F)).

(12) Etch of masking oxide (Fig. 3-1(G)) using buffer-HF from Transene Company

(13) Rinse in deionized (DI) water

(14) Photoresist strip (Fig. 3-1(H))

(15) Cleanup with organic solvents

(16) Polysilicon etch ($HF:HNO_3:H_2O$, 1:50:20) 2-4 min. (Fig. 3-1(I))

(17) Rinse in DI water

(18) Etch remaining masking oxide, buffer-HF etch for 3 min.

(19) Rinse in DI water and blow dry with nitrogen

(20) Dry oxidation at 1100°C, 24min., $t_{ox} = 0.1\mu m$ (Implant oxide Fig. 3-1(J))

(21) Blanket boron implant, 100 KeV, dose = $1 \times 10^{11} cm^{-2}$

(22) Cleanup with H_2SO_4

(23) Dehydration bake at 1100°C in nitrogen for 20 min.

(24) Photolithography, second mask, (source/drain implant level Fig. 3-1(K))

(25) Source/drain phosphorus implant, 90 KeV, dose = $1 \times 10^{14} cm^{-2}$

(26) Implant photoresist strip

(27) Cleanup with H_2SO_4

(28) Remove implant oxide using buffer-HF, 2 min.

(29) Rinse in DI water and blow dry with nitrogen

(30) Dry gate oxidation at 1100°C for 35 min., t_{ox} = 1000 Å (wafers D3 and D7 only)

(31) Steam gate oxidation at 900°C for 20 min., t_{ox} = 1000 Å (wafers D4 and D10 only)

(32) Photolithography, third mask, (contact window level)

(33) Open contact windows using buffer-HF, etch time=3 min.

(34) Rinse in DI water

(35) Photoresist strip

(36) Cleanup with HF.

(37) Aluminum deposition via evaporation (Fig. 3-1(L), 1 → 2 μm of very pure aluminum)

(38) Photolithography, fourth and final mask (aluminum interconnect level)

(39) Aluminum etch at 50°C using aluminum etchant – type A from Transene Company

(40) Rinse in DI water

(41) Photoresist strip (Fig. 3-1(M))

(42) Cleanup with organic solvents

(43) Optional 415°C 30 min. N_2 sinter

B.3. DETAILED PROCESS DESCRIPTION FOR WAFERS D29, D30, D31, D33, LI0A, 192

This section lists the process steps that were used to fabricate devices on substrate types C and D (Fig. 3-1(D) and Section 3.2). Wafers prefixed with a "D" are silicon substrates that were processed in parallel with the bubble substrates: LI0A and 192. The gas flow rate for all oxidations, steam and dry, was 1 liter per min. For the steam oxidations, we bubbled pure oxygen through DI water at 95°C and then fed this "wet" oxygen to the furnace tube. The lower thermal conductivity of bubble substrates with respect to silicon substrates mandated the use of longer wafer insertion/extraction times for all high temperature steps.

Step Number — Description

(1) Full cleanup (Fig. 3-1(A))

(2) Sputtered oxide deposition (spacer layer oxide $\sim$ 1 μm, Fig. 3-1(B))

(3) Cleanup with H_2SO_4

(4) Polysilicon deposition at 625°C, 0.75 μm (Fig. 3-1(C))

(5) Sputtered oxide deposition (3λ antireflection cap, Fig. 3-1(D))

(6) Laser recrystallization: bubble substrates at 0.7W, silicon substrates at 3.3W. Substrate temperature=400°C, scan speed=5 cm/sec.

(7) Cleanup with H_2SO_4

(8) Remove antireflection caps in HF (Fig. 3-1(E))

(9) Rinse in DI water

(10) Full cleanup

(11) Steam oxidation at 850°C for 120 min., t_{ox} = 1625 Å (masking oxide, Fig. 3-1(F))

(12) Photolithography, first mask, (silicon island definition level, Fig. 3-1(F))

(13) Etch of masking oxide (Fig. 3-1(G)) using buffer-HF from Transene Company

(14) Rinse in deionized (DI) water

(15) Photoresist strip (Fig. 3-1(H))

(16) Cleanup with organic solvents

(17) Polysilicon etch ($HF:HNO_3:H_2O$, 1:50:20) 2-4 min. (Fig. 3-1(I))

(18) Rinse in DI water

(19) Etch remaining masking oxide using TIMETCH from Transene Company. Time of etch=60-80 min. at 20°C

(20) Rinse in DI water and blow dry with nitrogen

(21) Steam oxidation at 850°C for 67 min., t_{ox} = 1000 Å (implant oxide Fig. 3-1(J))

(22) Blanket boron implant, 100 KeV, dose = $1 \times 10^{11} cm^{-2}$

(23) Cleanup with H_2SO_4

(24) Photolithography, second mask, (source/drain implant level Fig. 3-1(K))

(25) Source/drain phosphorus implant, 90 KeV, dose = $1 \times 10^{14} cm^{-2}$

(26) Implant photoresist strip

(27) Cleanup with H_2SO_4

(28) Remove implant oxide using TIMETCH, 40 min.

(29) Rinse in DI water and blow dry with nitrogen

(30) Steam gate oxidation at 850°C for 67 min., t_{ox} = 1000 Å

(31) Photolithography, third mask, (contact window level)

(32) Open contact windows using buffer-HF, etch time = 5 min.

(33) Rinse in DI water

(34) Photoresist strip

(35) Cleanup with HF

(36) Aluminum deposition via evaporation (Fig. 3-1(L), 1 → 2μm of pure aluminum)

(37) Photolithography, forth and final mask (aluminum interconnect level)

(38) Aluminum etch at 50°C using aluminum etchant-type A from Transene Company

(39) Rinse in DI water

(40) Photoresist strip (Fig. 3-1(M))

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Interim Report

16. Abstract

The feasibility of combining silicon and magnetic bubble technologies is demonstrated in this investigation. Results of the bubble film annealing portion of this work indicates that a low temperature silicon-on-garnet technology is the most likely one to succeed commercially. Long annealing times ($\geq$ 3 hrs.) at even moderate temperatures (~850°C) are highly undesirable; however, very short annealing times (20-600 μsec) at high temperatures (~1415°C) are less likely to have any adverse effect on the bubble film. The uniaxial magnetic anisotropy energy density (K_u) for some films is not even affected by such a fast anneal. Annealing ambients are also shown to have a major effect on the magnetic properties of bubble films. Functional MOSFETs have been fabricated on bubble films coated with thick (~1 μm) SiO_2 layers. The two main problems with these silicon-on-garnet MOSFETs are low electron mobilities and large gate leakage currents. The electron mobility for unsintered devices is 6±6cm^2/V-S with the gate leakage current being ~0.17μA at V_{DS} = 0 V and V_{GS} = 8 V. These results indicate that the laser recrystallized silicon and gate oxide (SiO_2) layers are contaminated; the data suggests that, part of the contaminating ions originate in the sputtered oxide spacer layer (this SiO_2 layer separates the silicon film from the bubble film), and part originate in the bubble film itself. A diffusion barrier, such as silicon nitride, placed between the bubble film and the silicon layer should eliminate the contamination induced problem. Of course, reducing process temperatures and times will also lower the levels of process induced contamination. In short, it appears that process optimization will lead to much improved silicon-on-garnet MOSFETs.

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